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Jameco Part Number 193341



PIC16C5X

EPROM/ROM-Based 8-Bit CMOS Microcontroller Series

Devices Included in this Data Sheet:

- PIC16C52
- PIC16C54s
- PIC16CR54s
- PIC16C55s
- PIC16C56s
- PIC16CR56s
- PIC16C57s
- PIC16CR57s
- PIC16C58s
- PIC16CR58s

Note: The letter "s" used following the part numbers throughout this document indicate plural, meaning there is more than one part variety for the indicated device.

High-Performance RISC CPU:

- · Only 33 single word instructions to learn
- All instructions are single cycle (200 ns) except for program branches which are two-cycle
- Operating speed: DC 20 MHz clock input DC - 200 ns instruction cycle

Device	Pins	I/O	EPROM/ ROM	RAM
PIC16C52	18	12	384	25
PIC16C54	18	12	512	25
PIC16C54A	18	12	512	25
PIC16C54B	18	12	512	25
PIC16CR54A	18	12	512	25
PIC16CR54B	18	12	512	25
PIC16C55	28	20	512	24
PIC16C55A	28	20	512	24
PIC16C56	18	12	1K	25
PIC16C56A	18	12	1K	25
PIC16CR56A	18	12	1K	25
PIC16C57	28	20	2K	72
PIC16C57C	28	20	2K	72
PIC16CR57B	28	20	2K	72
PIC16CR57C	28	20	2K	72
PIC16C58A	18	12	2K	73
PIC16C58B	18	12	2K	73
PIC16CR58A	18	12	2K	73
PIC16CR58B	18	12	2K	73

- 12-bit wide instructions
- 8-bit wide data path
- Seven or eight special function hardware registers
- Two-level deep hardware stack
- Direct, indirect and relative addressing modes for data and instructions

Peripheral Features:

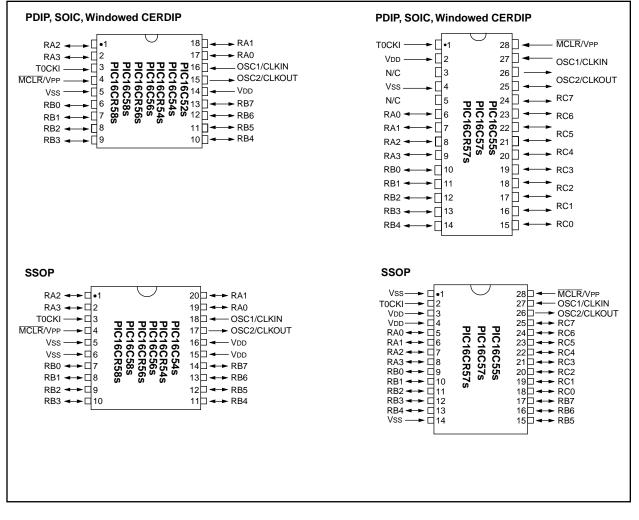
- · 8-bit real time clock/counter (TMR0) with 8-bit programmable prescaler
- Power-On Reset (POR)
- Device Reset Timer (DRT) ٠
- Watchdog Timer (WDT) with its own on-chip ٠ RC oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options: •
 - RC: Low-cost RC oscillator
 - XT: Standard crystal/resonator
 - HS: High-speed crystal/resonator -
 - LP: Power saving, low-frequency crystal

CMOS Technology:

- Low-power, high-speed CMOS EPROM/ROM technology
- · Fully static design
- Wide-operating voltage and temperature range:
 - EPROM Commercial/Industrial 2.0V to 6.25V
 - ROM Commercial/Industrial 2.0V to 6.25V
 - EPROM Extended 2.5V to 6.0V
 - ROM Extended 2.5V to 6.0V
- Low-power consumption
 - < 2 mA typical @ 5V, 4 MHz
 - 15 μA typical @ 3V, 32 kHz
 - < 0.6 μA typical standby current (with WDT disabled) @ 3V, 0°C to 70°C

Note: In this document, figure and table titles refer to all varieties of the part number indicated, (i.e., The title "Figure 14-1: Load Conditions - PIC16C54A", also refers to PIC16LC54A and PIC16LV54A parts).

Pin Diagrams



Device Voltag Range		Oscillator Selection (Program)	Oscillator	Process Technology (Microns)	ROM Equivalent	MCLR Filter
PIC16C52	3.0-6.25	User	See Note 1	0.9	—	No
PIC16C54	2.5-6.25	Factory	See Note 1	1.2	PIC16CR54A	No
PIC16C54A	2.0-6.25	User	See Note 1	0.9	_	No
PIC16C54B	3.0-5.5	User	See Note 1	0.7	PIC16CR54B	Yes
PIC16C55	2.5-6.25	Factory	See Note 1	1.7	—	No
PIC16C55A	3.0-5.5	User	See Note 1	0.7	_	Yes
PIC16C56	2.5-6.25	Factory	See Note 1	1.7	_	No
PIC16C56A	3.0-5.5	User	See Note 1	0.7	PIC16CR56A	Yes
PIC16C57	2.5-6.25	Factory	See Note 1	1.2	_	No
PIC16C57C	3.0-5.5	User	See Note 1	0.7	PIC16CR57C	Yes
PIC16CR57C	2.5-5.5	Factory	See Note 1	0.7	NA	Yes
PIC16C58A	2.0-6.25	User	See Note 1	0.9	PIC16CR58A	No ⁽²⁾
PIC16C58B	3.0-5.5	User	See Note 1	0.7	PIC16CR58B	Yes
PIC16CR54A	2.5-6.25	Factory	See Note 1	1.2	NA	Yes
PIC16CR54B	2.5-5.5	Factory	See Note 1	0.7	NA	Yes
PIC16CR56A	2.5-5.5	Factory	See Note 1	0.7	NA	Yes
PIC16CR57B	2.5-6.25	Factory	See Note 1	0.9	NA	Yes
PIC16CR58A	2.5-6.25	Factory	See Note 1	0.9	NA	Yes
PIC16CR58B	2.5-5.5	Factory	See Note 1	0.7	NA	Yes

Device Differences

Note 1: If you change from this device to another device, please verify oscillator characteristics in your application. **Note 2:** In PIC16LV58A, MCLR Filter = Yes

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1.0 GENERAL DESCRIPTION

The PIC16C5X from Microchip Technology is a family of low-cost, high performance, 8-bit, fully static, EPROM/ ROM-based CMOS microcontrollers. It employs a RISC architecture with only 33 single word/single cycle instructions. All instructions are single cycle (200 ns) except for program branches which take two cycles. The PIC16C5X delivers performance an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC16C5X products are equipped with special features that reduce system cost and power requirements. The Power-On Reset (POR) and Device Reset Timer (DRT) eliminate the need for external reset circuitry. There are four oscillator configurations to choose from, including the power-saving LP (Low Power) oscillator and cost saving RC oscillator. Power saving SLEEP mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The UV erasable CERDIP packaged versions are ideal for code development, while the cost-effective One Time Programmable (OTP) versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers while benefiting from the OTP's flexibility.

The PIC16C5X products are supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a 'C' compiler, fuzzy logic support tools, a low-cost development programmer, and a full featured programmer. All the tools are supported on $IBM^{\textcircled{B}}$ PC and compatible machines.

1.1 <u>Applications</u>

The PIC16C5X series fits perfectly in applications ranging from high-speed automotive and appliance motor control to low-power remote transmitters/receivers, pointing devices and telecom processors. The EPROM technology makes customizing application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make this microcontroller series perfect for applications with space limitations. Low-cost, low-power, high performance, ease of use and I/O flexibility make the PIC16C5X series very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic in larger systems, coprocessor applications).

TABLE 1-1: PIC16C5X FAMILY OF DEVICES

		PIC16C52	PIC16C54s	PIC16CR54s	PIC16C55s	PIC16C56s
Clock	Maximum Frequency of Operation (MHz)	4	20	20	20	20
	EPROM Program Memory (x12 words)	384	512	—	512	1K
Memory	ROM Program Memory (x12 words)	_	-	512		—
	RAM Data Memory (bytes)	25	25	25	24	25
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0
	I/O Pins	12	12	12	20	12
	Number of Instructions	33	33	33	33	33
Features	Packages	18-pin DIP, SOIC	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	28-pin DIP, SOIC; 28-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer (except PIC16C52), selectable code protect and high I/O current capability.

		PIC16CR56s	PIC16C57s	PIC16CR57s	PIC16C58s	PIC16CR58s
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20	20
	EPROM Program Memory (x12 words)	—	2К	-	2К	—
Memory	ROM Program Memory (x12 words)	1K		2К	-	2K
	RAM Data Memory (bytes)	25	72	72	73	73
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0
	I/O Pins	12	20	20	12	12
	Number of Instructions	33	33	33	33	33
Features	Packages	18-pin DIP, SOIC; 20-pin SSOP	28-pin DIP, SOIC; 28-pin SSOP	28-pin DIP, SOIC; 28-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP

All PIC16/17 Family devices have Power-on Reset, selectable Watchdog Timer (except PIC16C52), selectable code protect and high I/O current capability.

2.0 PIC16C5X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the PIC16C5X Product Identification System at the back of this data sheet to specify the correct part number.

For the PIC16C5X family of devices, there are four device types, as indicated in the device number:

- 1. **C**, as in PIC16C54. These devices have EPROM program memory and operate over the standard voltage range.
- 2. **LC**, as in PIC16LC54A. These devices have EPROM program memory and operate over an extended voltage range.
- 3. **LV**, as in PIC16LV54A. These devices have EPROM program memory and operate over a 2.0V to 3.8V range.
- 4. **CR**, as in PIC16CR54A. These devices have ROM program memory and operate over the standard voltage range.
- 5. **LCR**, as in PIC16LCR54B. These devices have ROM program memory and operate over an extended voltage range.

2.1 UV Erasable Devices (EPROM)

The UV erasable versions, offered in CERDIP packages, are optimal for prototype development and pilot programs

UV erasable devices can be programmed for any of the four oscillator configurations. Microchip's PICSTART[®] and PRO MATE[®] programmers both support programming of the PIC16C5X. Third party programmers also are available; refer to the Third Party Guide for a list of sources.

2.2 <u>One-Time-Programmable (OTP)</u> <u>Devices</u>

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must be programmed.

2.3 <u>Quick-Turnaround-Production (QTP)</u> <u>Devices</u>

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

2.4 <u>Serialized</u> <u>Quick-Turnaround-Production</u> (SQTP SM) Devices

Microchip offers the unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory.

Serial programming allows each device to have a unique number which can serve as an entry code, password or ID number.

2.5 Read Only Memory (ROM) Devices

Microchip offers masked ROM versions of several of the highest volume parts, giving the customer a low cost option for high volume, mature products. NOTES:

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C5X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C5X uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12-bits wide making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle (200ns @ 20MHz) except for program branches.

The PIC16C52 addresses 384 x 12 of program memory, the PIC16C54s/CR54s and PIC16C55s address 512 x 12 of program memory, the PIC16C56s/CR56s address 1K X 12 of program memory, and the PIC16C57s/CR57s and PIC16C58s/CR58s address 2K x 12 of program memory. All program memory is internal.

The PIC16C5X can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C5X has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C5X simple yet efficient. In addition, the learning curve is reduced significantly.

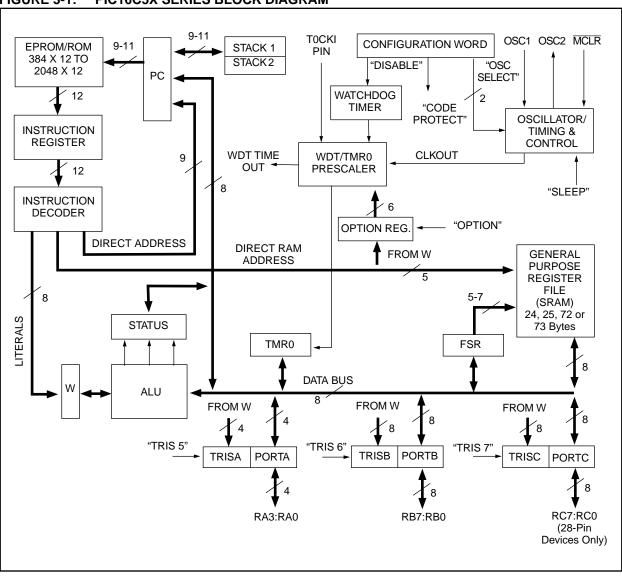
The PIC16C5X device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBWF and ADDWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1.





Name	DIP, SOIC No.	SSOP No.	I/O/P Type	Input Levels	Description
RA0	17	19	I/O	TTL	Bi-directional I/O port
RA1	18	20	I/O	TTL	
RA2	1	1	I/O	TTL	
RA3	2	2	I/O	TTL	
RB0	6	7	I/O	TTL	Bi-directional I/O port
RB1	7	8	I/O	TTL	
RB2	8	9	I/O	TTL	
RB3	9	10	I/O	TTL	
RB4	10	11	I/O	TTL	
RB5	11	12	I/O	TTL	
RB6	12	13	I/O	TTL	
RB7	13	14	I/O	TTL	
TOCKI	3	3	Ι	ST	Clock input to Timer0. Must be tied to Vss or VDD, if not in
					use, to reduce current consumption.
MCLR/Vpp	4	4	Ι	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device. Voltage on the MCLR/VPP pin must not exceed VDD to avoid unintended entering of programming mode.
OSC1/CLKIN	16	18	Ι	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	17	0		Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
Vdd	14	15,16	Р	_	Positive supply for logic and I/O pins.
Vss	5	5,6	Р	_	Ground reference for logic and I/O pins.

TABLE 3-1:PINOUT DESCRIPTION - PIC16C52, PIC16C54s, PIC16CR54s, PIC16C56s,
PIC16CR56s, PIC16CR58s, PIC16CR58s

Legend: I = input, O = output, I/O = input/output,

P = power, — = Not Used, TTL = TTL input,

ST = Schmitt Trigger input

TABLE 3-2:PINOUT DESCRIPTION -PIC16C55s, PIC16C57s, PIC16CR57s

Name	DIP, SOIC No.	SSOP No.	I/O/P Type	Input Levels	Description
RA0	6	5	I/O	TTL	Bi-directional I/O port
RA1	7	6	I/O	TTL	
RA2	8	7	I/O	TTL	
RA3	9	8	I/O	TTL	
RB0	10	9	I/O	TTL	Bi-directional I/O port
RB1	11	10	I/O	TTL	
RB2	12	11	I/O	TTL	
RB3	13	12	I/O	TTL	
RB4	14	13	I/O	TTL	
RB5	15	15	I/O	TTL	
RB6	16	16	I/O	TTL	
RB7	17	17	I/O	TTL	
RC0	18	18	I/O	TTL	Bi-directional I/O port
RC1	19	19	I/O	TTL	
RC2	20	20	I/O	TTL	
RC3	21	21	I/O	TTL	
RC4	22	22	I/O	TTL	
RC5	23	23	I/O	TTL	
RC6	24	24	I/O	TTL	
RC7	25	25	I/O	TTL	
TOCKI	1	2	I	ST	Clock input to Timer0. Must be tied to Vss or VDD if not in use to reduce current consumption.
MCLR	28	28	I	ST	Master clear (reset) input. This pin is an active low reset to the device.
OSC1/CLKIN	27	27	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	26	26	0	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
Vdd	2	3,4	Р		Positive supply for logic and I/O pins.
Vss	4	1,14	Р		Ground reference for logic and I/O pins.
N/C	3,5				Unused, do not connect

Legend: I = input, O = output, I/O = input/output,

P = power, — = Not Used,

TTL = TTL input, ST = Schmitt Trigger input

3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter is incremented every Q1, and the instruction is fetched from program memory and latched into instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2 and Example 3-1.

3.2 Instruction Flow/Pipelining

An Instruction Cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO) then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

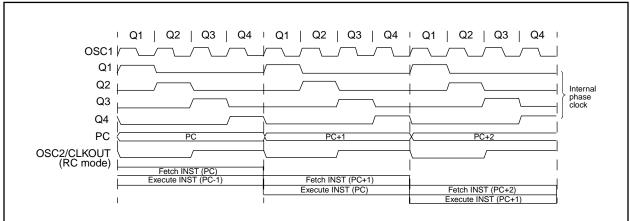
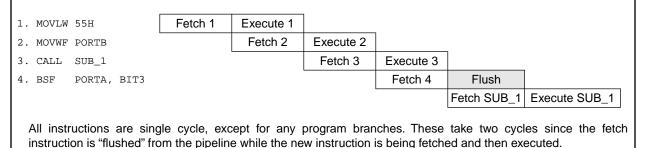


FIGURE 3-2: CLOCK/INSTRUCTION CYCLE

EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



NOTES:

4.0 MEMORY ORGANIZATION

PIC16C5X memory is organized into program memory and data memory. For devices with more than 512 bytes of program memory, a paging scheme is used. Program memory pages are accessed using one or two STATUS register bits. For devices with a data memory register file of more than 32 registers, a banking scheme is used. Data memory banks are accessed using the File Selection Register (FSR).

4.1 Program Memory Organization

The PIC16C52 has a 9-bit Program Counter (PC) capable of addressing a 384 x 12 program memory space (Figure 4-1). The PIC16C54s, PIC16CR54s and PIC16C55s have a 9-bit Program Counter (PC) capable of addressing a 512 x 12 program memory space (Figure 4-2). The PIC16C56s and PIC16CR56s have a 10-bit Program Counter (PC) capable of addressing a 1K x 12 program memory space (Figure 4-3). The PIC16CR57s, PIC16C58s and PIC16CR58s have an 11-bit Program Counter capable of addressing a 2K x 12 program memory space (Figure 4-4). Accessing a location above the physically implemented address will cause a wraparound.

The reset vector for the PIC16C52 is at 17Fh. A NOP at the reset vector location will cause a restart at location 000h. The reset vector for the PIC16C54s, PIC16CR54s and PIC16C55s is at 1FFh. The reset vector for the PIC16C56s and PIC16CR56s is at 3FFh. The reset vector for the PIC16C57s, PIC16CR57s, PIC16C58s, and PIC16CR58s is at 7FFh.

FIGURE 4-1: PIC16C52 PROGRAM MEMORY MAP AND STACK

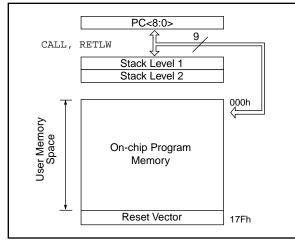


FIGURE 4-2: PIC16C54s/CR54s/C55s PROGRAM MEMORY MAP AND STACK

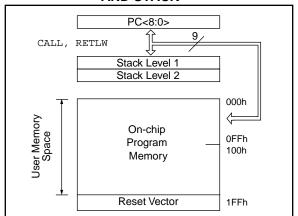


FIGURE 4-3: PIC16C56s/CR56s PROGRAM MEMORY MAP AND STACK

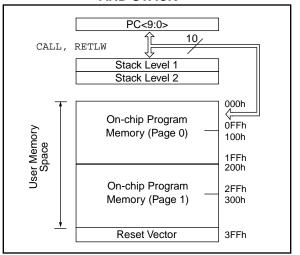
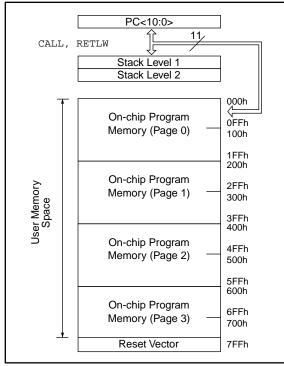


FIGURE 4-4: PIC16C57s/CR57s/C58s/ CR58s PROGRAM MEMORY MAP AND STACK



4.2 Data Memory Organization

Data memory is composed of registers, or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: special function registers and general purpose registers.

The special function registers include the TMR0 register, the Program Counter (PC), the Status Register, the I/O registers (ports), and the File Select Register (FSR). In addition, special purpose registers are used to control the I/O port configuration and prescaler options.

The general purpose registers are used for data and control information under command of the instructions.

For the PIC16C52, PIC16C54s, PIC16CR54s, PIC16C56s and PIC16CR56s, the register file is composed of 7 special function registers and 25 general purpose registers (Figure 4-5).

For the PIC16C55s, the register file is composed of 8 special function registers and 24 general purpose registers.

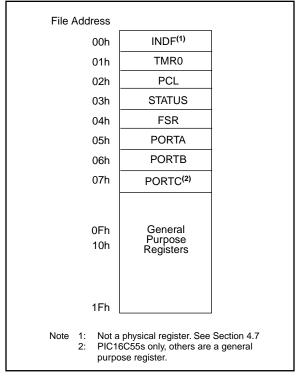
For the PIC16C57s and PIC16CR57s, the register file is composed of 8 special function registers, 24 general purpose registers and up to 48 additional general purpose registers that may be addressed using a banking scheme (Figure 4-6).

For the PIC16C58s and PIC16CR58s, the register file is composed of 7 special function registers, 25 general purpose registers and up to 48 additional general purpose registers that may be addressed using a banking scheme (Figure 4-7).

4.2.1 GENERAL PURPOSE REGISTER FILE

The register file is accessed either directly or indirectly through the file select register FSR (Section 4.7).

FIGURE 4-5: PIC16C52, PIC16C54s, PIC16CR54s, PIC16C55s, PIC16C56s, PIC16CR56s REGISTER FILE MAP



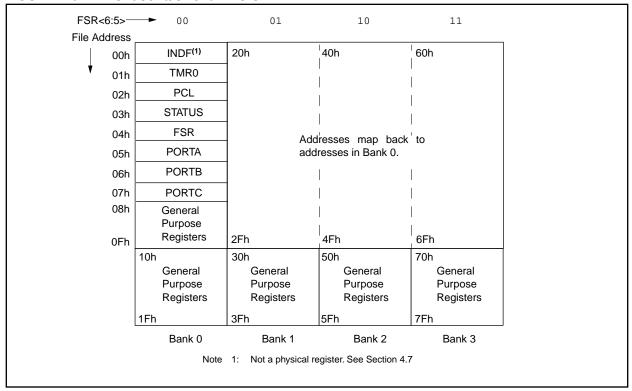
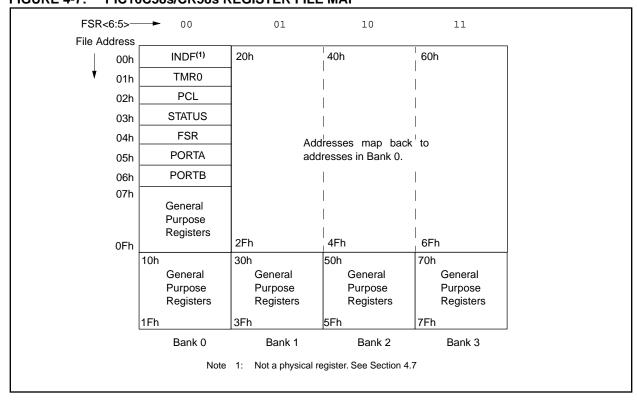


FIGURE 4-7: PIC16C58s/CR58s REGISTER FILE MAP



4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device (Table 4-1). The special registers can be classified into two sets. The special function registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

TABLE 4-1:SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on MCLR and WDT Reset
N/A	TRIS	I/O cont	rol registe	ers (TRIS/	A, TRISB,	TRISC)				1111 1111	1111 1111
N/A	OPTION	Contains	s control b	oits to cor	ifigure Tir	ner0 and	Timer0/W	DT presc	aler	11 1111	11 1111
00h	INDF	Uses co	ntents of	egister)	xxxx xxxx	uuuu uuuu					
01h	TMR0	8-bit rea	I-time clo		xxxx xxxx	uuuu uuuu					
02h ⁽¹⁾	PCL	Low ord	er 8 bits c	of PC						1111 1111	1111 1111
03h	STATUS	PA2	PA1	PA0	TO	PD	Z	DC	С	0001 1xxx	000q quuu
04h	FSR	Indirect	data men	nory addre	ess pointe	er				1xxx xxxx	luuu uuuu
05h	PORTA	—	—	—		RA3	RA2	RA1	RA0	xxxx	uuuu
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
07h ⁽²⁾	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu

Legend: Shaded boxes = unimplemented or unused, – = unimplemented, read as '0' (if applicable) x = unknown, u = unchanged, q = see the tables in Section 7.7 for possible values.

Note 1: The upper byte of the Program Counter is not directly accessible. See Section 4.5

for an explanation of how to access these bits.

2: File address 07h is a general purpose register on the PIC16C52, PIC16C54s, PIC16CR54s, PIC16C56s, PIC16CR56s, PIC16C58s and PIC16CR58s.

4.3 STATUS Register

Г

This register contains the arithmetic status of the ALU, the RESET status, and the page preselect bits for program memories larger than 512 words.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the \overline{TO} and \overline{PD} bits are

not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS register as 000u uluu (where u = unchanged).

It is recommended, therefore, that only BCF, BSF and MOVWF instructions be used to alter the STATUS register because these instructions do not affect the Z, DC or C bits from the STATUS register. For other instructions, which do affect STATUS bits, see Section 8.0, Instruction Set Summary.

FIGURE 4-8: STATUS REGISTER (ADDRESS:03h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x	
PA2	PA1	PA0	TO	PD	Z	DC	С	R = Readable bit
bit7	6	5	4	3	2	1	bit0	W = Writable bit - n = Value at POR reset
bit 7:	PA2: This b Use of the compatibilit	PA2 bit as a	a general p	ourpose read	d/write bit is	not recomm	ended, since	e this may affect upward
bit 6-5:	00 = Page 01 = Page 10 = Page 11 = Page Each page Using the F	0 (000h - 1 1 (200h - 3 2 (400h - 5 3 (600h - 7 is 512 wor PA1:PA0 bit	FFh) - PIC FFh) - PIC FFh) - PIC FFh) - PIC ds. s as gener	16C56s/CR 16C56s/CR 16C57s/CR 16C57s/CR al purpose r	56s, PIC16C 56s, PIC16C 57s, PIC16C 57s, PIC16C 57s, PIC16C	57s/CR57s 57s/CR57s 58s/CR58s 58s/CR58s s in devices	, PIC16C58s , PIC16C58s s which do no	
bit 4:	TO : Time-or 1 = After po 0 = A WDT	ower-up, CI		ruction, or s	LEEP instruc	tion		
bit 3:	PD : Power- 1 = After po 0 = By exec	ower-up or		WDT instruc struction	tion			
bit 2:				logic opera logic opera	tion is zero tion is not ze	ro		
bit 1:	ADDWF 1 = A carry 0 = A carry SUBWF 1 = A borro	from the 4 from the 4 w from the 4	th low orde th low orde 4th low ord	er bit of the r er bit of the r der bit of the	BWF instructi esult occurre esult did not e result did n e result occu	ed occur ot occur		
bit 0:	C: Carry/bo	orrow bit (fo	r addwf, s	UBWF and R SUBWF	RF, RLF insti	uctions)	RRF or R	
	1 = A carry	occurred	cur	1 = A bor	row did not o			<pre>with LSb or MSb, respectively</pre>

By executing the <code>OPTION</code> instruction, the contents of the W register will be transferred to the <code>OPTION</code>

register. A RESET sets the OPTION<5:0> bits.

4.4 OPTION Register

The OPTION register is a 6-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

FIGURE 4-9: OPTION REGISTER

U-0 U-0 W-1 W-1 W-1 W-1 W-1 W-1 T0CS T0SE PSA PS2 PS1 PS0 W = Writable bit U = Unimplemented bit 2 bit7 6 5 4 3 1 bit0 - n = Value at POR reset bit 7-6: Unimplemented. bit 5: TOCS: Timer0 clock source select bit 1 = Transition on TOCKI pin 0 = Internal instruction cycle clock (CLKOUT) bit 4: T0SE: Timer0 source edge select bit 1 = Increment on high-to-low transition on T0CKI pin 0 = Increment on low-to-high transition on T0CKI pin bit 3: PSA: Prescaler assignment bit 1 = Prescaler assigned to the WDT (not implemented on PIC16C52) 0 = Prescaler assigned to Timer0 bit 2-0: PS2:PS0: Prescaler rate select bits Timer0 Rate WDT Rate (not implemented on PIC16C52) Bit Value 000 1:2 1:1 001 1:4 1:2 010 1:8 1:4 011 1:16 1:8 100 1:32 1:16 101 1:64 1:32 1:64 110 1:128 111 1:256 1:128

4.5 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

For a GOTO instruction, bits 8:0 of the PC are provided by the GOTO instruction word. The PC Latch (PCL) is mapped to PC<7:0> (Figure 4-10 and Figure 4-11).

For the PIC16C56s, PIC16CR56s, PIC16C57s, PIC16CR57s, PIC16CR57s, PIC16C58s and PIC16CR58s, a page number must be supplied as well. Bit5 and bit6 of the STATUS register provide page information to bit9 and bit10 of the PC (Figure 4-11 and Figure 4-12).

For a CALL instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-10 and Figure 4-11).

Instructions where the PCL is the destination, or Modify PCL instructions, include MOVWF PC, ADDWF PC, and BSF PC, 5.

For the PIC16C56s, PIC16CR56s, PIC16C57s, PIC16CR57s, PIC16CR57s, PIC16C58s and PIC16CR58s, a page number again must be supplied. Bit5 and bit6 of the STATUS register provide page information to bit9 and bit10 of the PC (Figure 4-11 and Figure 4-12).

Note: Because PC<8> is cleared in the CALL instruction, or any Modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-10: LOADING OF PC BRANCH INSTRUCTIONS -PIC16C52, PIC16C54s, PIC16CR54s, PIC16C55s

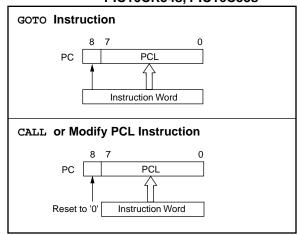
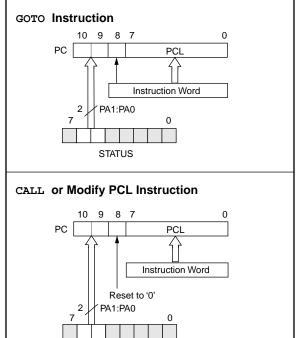
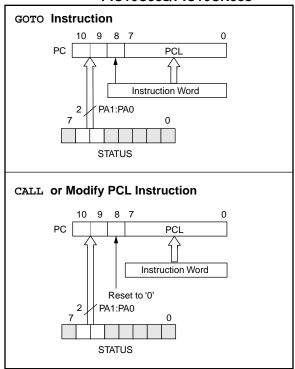


FIGURE 4-11: LOADING OF PC BRANCH INSTRUCTIONS -PIC16C56s/PIC16CR56s



STATUS

FIGURE 4-12: LOADING OF PC BRANCH INSTRUCTIONS -PIC16C57s/PIC16CR57s, AND PIC16C58s/PIC16CR58s



For the RETLW instruction, the PC is loaded with the Top Of Stack (TOS) contents. All of the devices covered in this data sheet have a two-level stack. The stack has the same bit width as the device PC. 4.5.1 PAGING CONSIDERATIONS – PIC16C56s/CR56s, PIC16C57s/CR57s AND PIC16C58s/CR58s

If the Program Counter is pointing to the last address of a selected memory page, when it increments it will cause the program to continue in the next higher page. However, the page preselect bits in the STATUS register will not be updated. Therefore, the next GOTO, CALL, or Modify PCL instruction will send the program to the page specified by the page preselect bits (PA0 or PA1:PA0).

For example, a NOP at location 1FFh (page 0) increments the PC to 200h (page 1). A GOTO xxx at 200h will return the program to address xxxh on page 0 (assuming that PA1:PA0 are clear).

To prevent this, the page preselect bits must be updated under program control.

4.5.2 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page i.e., the reset vector.

The STATUS register page preselect bits are cleared upon a RESET, which means that page 0 is pre-selected.

Therefore, upon a RESET, a GOTO instruction at the reset vector location will automatically cause the program to jump to page 0.

4.6 Stack

PIC16C5X devices have a 9-bit, 10-bit or 11-bit wide, two-level hardware push/pop stack (Figure 4-2, Figure 4-1, and Figure 4-3 respectively).

A CALL instruction will *push* the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential CALL's are executed, only the most recent two return addresses are stored.

A RETLW instruction will *pop* the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential RETLW's are executed, the stack will be filled with the address previously stored in level 2. Note that the W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

4.7 Indirect Data Addressing; INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 4-1: INDIRECT ADDRESSING

- Register file 05 contains the value 10h
- Register file 06 contains the value 0Ah
- · Load the value 05 into the FSR register
- A read of the INDF register will return the value of 10h
- Increment the value of the FSR register by one (FSR = 06)
- A read of the INDR register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although STATUS bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 4-2.

EXAMPLE 4-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

	movlw	0x10	;initialize pointer
	movwf	FSR	; to RAM
NEXT	clrf	INDF	clear INDF register;
	incf	FSR,F	;inc pointer
	btfsc	FSR,4	;all done?
	goto	NEXT	;NO, clear next
CONTINUE			
	:		;YES, continue

The FSR is either a 5-bit (PIC16C52, PIC16C54s, PIC16CR54s, PIC16CR54s, PIC16C55s), 6-bit (PIC16C56s, PIC16CR56s), or 7-bit (PIC16C57s, PIC16CR57s, PIC16CR58s) wide register. It is used in conjunction with the INDF register to indirectly address the data memory area.

The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

PIC16C52, PIC16C54s, PIC16CR54s, PIC16C55s: Do not use banking. FSR<6:5> are unimplemented and read as '1's.

PIC16C56s, PIC16CR56s: FSR<6:5> are the bank select bits and are used to select the bank to be addressed (00 = bank 0, 01 = bank 1, 10 = invalid, 11 = invalid).

PIC16C57s, **PIC16CR57s**, **PIC16C58s**, **PIC16CR58s**: FSR<6:5> are the bank select bits and are used to select the bank to be addressed (00 = bank 0, 01 = bank 1, 10 = bank 2, 11 = bank 3).

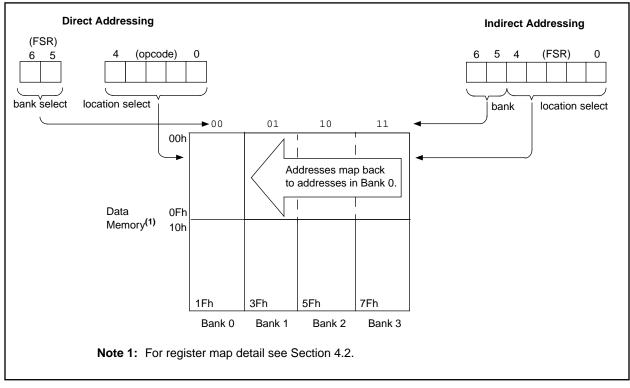


FIGURE 4-13: DIRECT/INDIRECT ADDRESSING

Vdd

N

Vss

I/O

pin⁽¹⁾

5.0 I/O PORTS

As with any other register, the I/O registers can be written and read under program control. However, read instructions (e.g., MOVF PORTB, W) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers (TRISA, TRISB, TRISC) are all set.

5.1 <u>PORTA</u>

PORTA is a 4-bit I/O register. Only the low order 4 bits are used (RA3:RA0). Bits 7-4 are unimplemented and read as '0's.

5.2 <u>PORTB</u>

PORTB is an 8-bit I/O register (PORTB<7:0>).

5.3 <u>PORTC</u>

PORTC is an 8-bit I/O register for PIC16C55s, PIC16C57s and PIC16CR57s.

PORTC is a general purpose register for PIC16C52, PIC16C54s, PIC16CR54s, PIC16C56s, PIC16C58s and PIC16CR58s.

5.4 TRIS Registers

The output driver control registers are loaded with the contents of the W register by executing the TRIS f instruction. A '1' from a TRIS register bit puts the corresponding output driver in a hi-impedance mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer.

Note:	A read of the ports reads the pins, not the output data latches. That is, if an output
	driver on a pin is enabled and driven high,
	but the external system is holding it low, a
	read of the port will indicate that the pin is
	low.

The TRIS registers are "write-only" and are set (output drivers disabled) upon RESET.

TABLE 5-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on MCLR and WDT Reset
N/A	TRIS	I/O conti	ol registe	ers (TRISA	A, TRISB)					1111 1111	1111 1111
05h	PORTA	—	_	_	—	RA3	RA2	RA1	RA0	xxxx	uuuu
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu

5.5

FIGURE 5-1:

D

CK

D

CK

Data

Latch

TRIS

Latch

Reset

Data

Bus

WR

Port

W Reg

TRIS 'f'

I/O Interfacing

The equivalent circuit for an I/O port pin is shown in

Figure 5-1. All ports may be used for both input and

output operation. For input operations these ports are

non-latching. Any input must be present until read by

an input instruction (e.g., MOVF PORTB, W). The

outputs are latched and remain unchanged until the

output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA,

TRISB) must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin can

EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN

be programmed individually as input or output.

Q

Q

Q

 \overline{O}

RD Port

Note 1: I/O pins have protection diodes to VDD and Vss.

Legend: Shaded boxes = unimplemented, read as '0',

- = unimplemented, read as '0', x = unknown, u = unchanged

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5.6 I/O Programming Considerations

5.6.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Example 5-1 shows the effect of two sequential read-modify-write instructions (e.g., ${\rm BCF}\,,~{\rm BSF},~{\rm etc.})$ on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

;							
	BCF	PORTB,	7	;01pp	pppp	11pp	pppp
	BCF	PORTB,	6	;10pp	pppp	11pp	pppp
	MOVLW	03Fh		;			
	TRIS	PORTB		;10pp	pppp	10pp	pppp
;							

;Note that the user may have expected the pin ;values to be 00pp pppp. The 2nd BCF caused ;RB7 to be latched as the pin value (High).

5.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

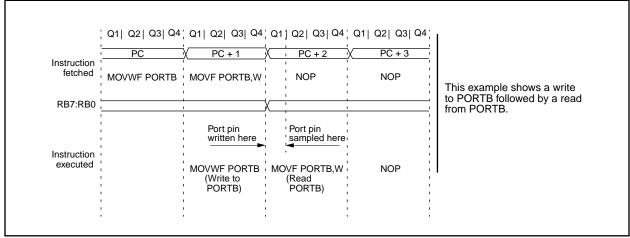


FIGURE 5-2: SUCCESSIVE I/O OPERATION

6.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
 - Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
 - Edge select for external clock

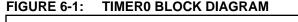
Figure 6-1 is a simplified block diagram of the Timer0 module, while Figure 6-2 shows the electrical structure of the Timer0 input.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 6-3 and Figure 6-4). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The incrementing edge is determined by the source edge select bit T0SE (OPTION<4>). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.1.

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. Section 6.2 details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 6-1.



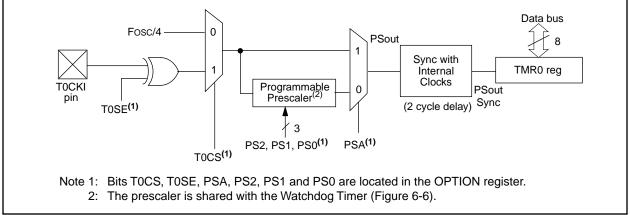
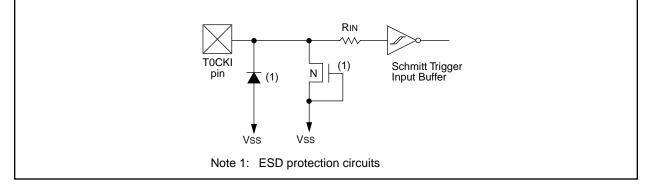


FIGURE 6-2: ELECTRICAL STRUCTURE OF TOCKI PIN





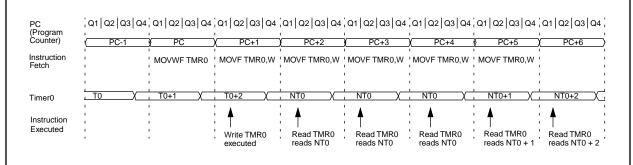


FIGURE 6-4: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

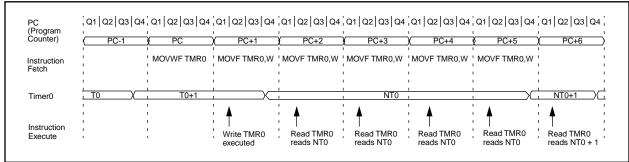


TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on MCLR and WDT Reset
01h	TMR0	Timer0	Timer0 - 8-bit real-time clock/counter							xxxx xxxx	uuuu uuuu
N/A	OPTION	—	—	TOCS	TOSE	PSA	PS2	PS1	PS0	11 1111	11 1111

Legend: Shaded cells: Unimplemented bits,

- = unimplemented, x = unknown, u = unchanged,

6.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

6.1.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device. When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for TOCKI to have a period of at least 4TOSC (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on TOCKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

6.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 6-5 shows the delay from the external clock edge to the timer incrementing.

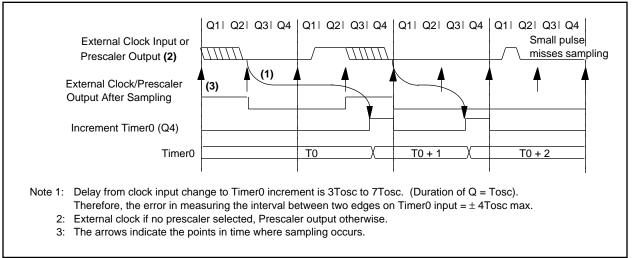


FIGURE 6-5: TIMER0 TIMING WITH EXTERNAL CLOCK

6.2 <u>Prescaler</u>

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer (WDT) (WDT postscaler not implemented on PIC16C52), respectively (Section 6.1.2). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS2:PS0 bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, x, etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a RESET, the prescaler contains all '0's.

6.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on the fly" during program execution). To avoid an unintended device RESET, the

following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 6-1:	CHANGING PRESCALER
	(TIMER0→WDT)

	•	
1.CLRWDT		;Clear WDT
2.CLRF	TMR0	;Clear TMR0 & Prescaler
3.MOVLW	'00xx1111 <i>'</i> b	;These 3 lines (5, 6, 7)
4.OPTION		; are required only if
		; desired
5.CLRWDT		;PS<2:0> are 000 or 001
6.MOVLW	'00xx1xxx'b	;Set Postscaler to
7.OPTION		; desired WDT rate

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 6-2. This sequence must be used even if the WDT is disabled. A CLRWDT instruction should be executed before switching the prescaler.

EXAMPLE 6-2: CHANGING PRESCALER (WDT \rightarrow TIMER0)

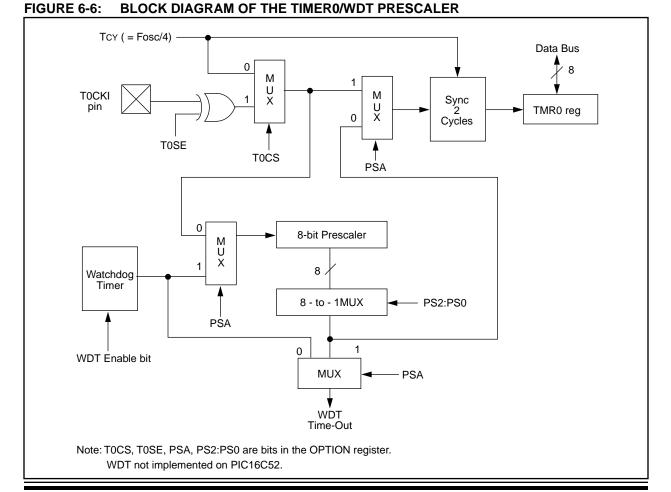
CLRWDT

'xxxx0xxx'

;Clear WDT and ;prescaler ;Select TMR0, new ;prescale value and ;clock source

OPTION

MOVIW



7.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of real-time applications. The PIC16C5X family of microcontrollers has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- · Oscillator selection
- Reset
- Power-On Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) (not implemented on PIC16C52)
- SLEEP
- · Code protection
- ID locations (not implemented on PIC16C52)

The PIC16C5X Family has a Watchdog Timer which can be shut off only through configuration bit WDTE. It runs off of its own RC oscillator for added reliability. There is an 18 ms delay provided by the Device Reset Timer (DRT), intended to keep the chip in reset until the crystal oscillator is stable. With this timer on-chip, most applications need no external reset circuitry. The SLEEP mode is designed to offer a very low current power-down mode. The user can wake up from SLEEP through external reset or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

7.1 Configuration Bits

Configuration bits can be programmed to select various device configurations. Two bits are for the selection of the oscillator type and one bit is the Watchdog Timer enable bit. Nine bits are code protection bits (Figure 7-1 and Figure 7-2) for the PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16CR58, and PIC16CR58 devices.

QTP or ROM devices have the oscillator configuration programmed at the factory and these parts are tested accordingly (see "Product Identification System" diagrams in the back of this data sheet).

FIGURE 7-1: CONFIGURATION WORD FOR PIC16CR54A/C54B/CR54B/C56A/CR56A/CR57B/C58B/CR58A/CR58B

CP	CP	CP	CP	CP	CP	CP	CP	CP	WDTE	FOSC1	FOSC0	Register:	CONFIG
bit11	10	9	8	7	6	5	4	3	2	1	bit0	Address ⁽¹⁾ :	FFFh
bit 11-3:	1 = Co	CP: Code protection bits 1 = Code protection off 0 = Code protection on											
bit 2:	1 = W	WDTE: Watchdog timer enable bit 1 = WDT enabled 0 = WDT disabled											
bit 1-0:	FOSC1:FOSC0: Oscillator selection bits 11 = RC oscillator 10 = HS oscillator 01 = XT oscillator 00 = LP oscillator												
Note 1:		Refer to the PIC16C5X Programming Specification (Literature Number DS30190) to deter- mine how to access the configuration word.											

FIGURE 7-2: CONFIGURATION WORD FOR PIC16C52/C54/C54A/C55/C56/C57/C58A

—	—	—	—	—	—	—		CP	WDTE	FOSC1	FOSC0	Register:	CONFIG
bit11	10	9	8	7	6	5	4	3	2	1	bit0	Address ⁽¹⁾ :	FFF
bit 11-4:	Unimp	lemente	ed: Read	as '0'									
bit 3:	1 = Co	CP: Code protection bit. 1 = Code protection off 0 = Code protection on											
bit 2:	1 = WI	WDTE: Watchdog timer enable bit (not implemented on PIC16C52) 1 = WDT enabled D = WDT disabled											
bit 1-0:	FOSC1:FOSC0: Oscillator selection bits ⁽²⁾ 11 = RC oscillator 10 = HS oscillator 01 = XT oscillator 00 = LP oscillator												
	00 = LP oscillator Refer to the PIC16C5X Programming Specifications (Literature Number DS30190) to determine how to access the configuration word. PIC16C52 supports XT and RC oscillator only. PIC16LV54A supports XT, RC and LP oscillator only. PIC16LV58A supports XT, RC and LP oscillator only.									Ö			

7.2 Oscillator Configurations

7.2.1 OSCILLATOR TYPES

PIC16C5Xs can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:

- LP: Low Power Crystal
- XT: Crystal/Resonator
- HS: High Speed Crystal/Resonator
- RC: Resistor/Capacitor

Note:	Not all oscillator selections available for all
	parts. See Section 7.1.

7.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 7-3). The PIC16C5X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source drive the OSC1/CLKIN pin (Figure 7-4).

FIGURE 7-3: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)

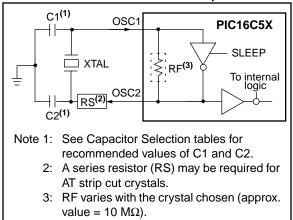


FIGURE 7-4: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

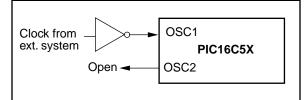


TABLE 7-1:	CAPACITOR SELECTION
	FOR CERAMIC RESONATORS
	- PIC16C5X, PIC16CR5X

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
XT	455 kHz	22-100 pF	22-100 pF
	2.0 MHz	15-68 pF	15-68 pF
	4.0 MHz	15-68 pF	15-68 pF
HS	4.0 MHz	15-68 pF	15-68 pF
	8.0 MHz	10-68 pF	10-68 pF
	16.0 MHz	10-22 pF	10-22 pF

These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 7-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR - PIC16C5X, PIC16CR5X

Osc Type	Resonator Freq	Cap.Range C1	Cap. Range C2
LP	32 kHz ⁽¹⁾	15 pF	15 pF
	100 kHz	15-30 pF	30-47 pF
	200 kHz	15-30 pF	15-82 pF
XT	100 kHz	15-30 pF	200-300 pF
	200 kHz	15-30 pF	100-200 pF
	455 kHz	15-30 pF	15-100 pF
	1 MHz	15-30 pF	15-30 pF
	2 MHz	15-30 pF	15-30 pF
	4 MHz	15-47 pF	15-47 pF
HS	4 MHz	15-30 pF	15-30 pF
	8 MHz	15-30 pF	15-30 pF
	20 MHz	15-30 pF	15-30 pF

Note 1: For VDD > 4.5V, C1 = C2 \approx 30 pF is recommended.

These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

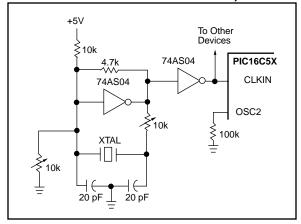
Note: If you change from this device to another device, please verify oscillator characteristics in your application.

7.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator or a simple oscillator circuit with TTL gates can be used as an external crystal oscillator circuit. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with parallel resonance, or one with series resonance.

Figure 7-5 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 k Ω resistor provides the negative feedback for stability. The 10 k Ω potentiometers bias the 74AS04 in the linear region. This circuit could be used for external oscillator designs.

FIGURE 7-5: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT (USING XT, HS OR LP OSCILLATOR MODE)



Note: If you change from this device to another device, please verify oscillator characteristics in your application.

This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 Ω resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 7-6: **EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT** (USING XT, HS OR LP **OSCILLATOR MODE)** To Other Devices 330 330 74AS04 PIC16C5X 74AS04 74AS04 CLKIN ┣┥ (-́┣ 0.1 μF OSC2 XTAL Ş 100k

Note: If you change from this device to another device, please verify oscillator characteristics in your application.

7.2.4 RC OSCILLATOR

For timing insensitive applications, the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used.

Figure 7-7 shows how the R/C combination is connected to the PIC16C5X. For Rext values below 2.2 k Ω , the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g., 1 M Ω) the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping Rext between 3 k Ω and 100 k Ω .

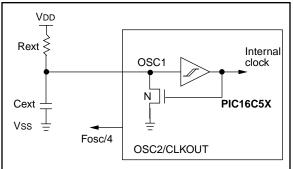
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

The Electrical Specifications sections show RC frequency variation from part to part due to normal process variation.

Also, see the Electrical Specifications sections for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic.

FIGURE 7-7: RC OSCILLATOR MODE



Note: If you change from this device to another device, please verify oscillator characteristics in your application.

7.3 <u>Reset</u>

PIC16C5X devices may be reset in one of the following ways:

- Power-On Reset (POR)
- MCLR reset (normal operation)
- MCLR wake-up reset (from SLEEP)
- WDT reset (normal operation)
- WDT wake-up reset (from SLEEP)

Table 7-3 shows these reset conditions for the PCL and STATUS registers.

Some registers are not affected in any reset condition. Their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset state" on Power-On Reset (POR), MCLR or WDT reset. A MCLR or WDT wake-up from SLEEP also results in a device reset, and not a continuation of operation before SLEEP.

The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits (STATUS <4:3>) are set or cleared depending on the different reset conditions (Section 7.7). These bits may be used to determine the nature of the reset.

Table 7-4 lists a full description of reset states of all registers. Figure 7-8 shows a simplified block diagram of the on-chip reset circuit.

TABLE 7-3: RESET CONDITIONS FOR SPECIAL REGISTERS

Condition	PCL Addr: 02h	STATUS Addr: 03h
Power-On Reset	1111 1111	0001 1xxx
MCLR reset (normal operation)	1111 1111	000u uuuu (1)
MCLR wake-up (from SLEEP)	1111 1111	0001 Ouuu
WDT reset (normal operation)	1111 1111	0000 luuu (2)
WDT wake-up (from SLEEP)	1111 1111	0000 Ouuu

Legend: u = unchanged, x = unknown, - = unimplemented read as '0'.

Note 1: TO and PD bits retain their last value until one of the other reset conditions occur.

2: The CLRWDT instruction will set the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits.

TABLE 7-4: RESET CONDITIONS FOR ALL REGISTERS

Register	Address	Power-On Reset	MCLR or WDT Reset
W	N/A	xxxx xxxx	นนนน นนนน
TRIS	N/A	1111 1111	1111 1111
OPTION	N/A	11 1111	11 1111
INDF	00h	XXXX XXXX	uuuu uuuu
TMR0	01h	XXXX XXXX	uuuu uuuu
PCL ⁽¹⁾	02h	1111 1111	1111 1111
STATUS ⁽¹⁾	03h	0001 1xxx	000q quuu
FSR	04h	1xxx xxxx	luuu uuuu
PORTA	05h	xxxx	uuuu
PORTB	06h	XXXX XXXX	uuuu uuuu
PORTC ⁽²⁾	07h	xxxx xxxx	uuuu uuuu
General Purpose Register Files	07-7Fh	xxxx xxxx	นนนน นนนน

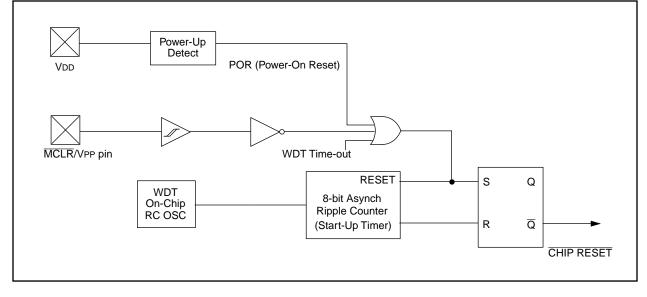
Legend: u = unchanged, x = unknown, - = unimplemented, read as '0',

q = see tables in Section 7.7 for possible values.

Note 1: See Table 7-3 for reset value for specific conditions.

2: General purpose register file on PIC16C52/C54s/CR54s/C56s/CR56s/C58s/CR58s

FIGURE 7-8: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



7.4 Power-On Reset (POR)

The PIC16C5X family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip reset for most power-up situations. To use this feature, the user merely ties the MCLR/VPP pin to VDD. A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 7-8.

The Power-On Reset circuit and the Device Reset Timer (Section 7.5) circuit are closely related. On power-up, the reset latch is set and the DRT is reset. The DRT timer begins counting once it detects $\overline{\text{MCLR}}$ to be high. After the time-out period, which is typically 18 ms, it will reset the reset latch and thus end the on-chip reset signal.

A power-up example where $\overline{\text{MCLR}}$ is not tied to VDD is shown in Figure 7-10. VDD is allowed to rise and stabilize before bringing $\overline{\text{MCLR}}$ high. The chip will actually come out of reset TDRT msec after $\overline{\text{MCLR}}$ goes high.

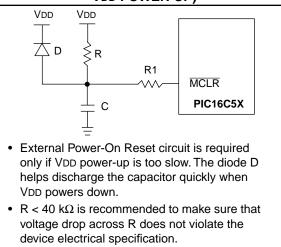
In Figure 7-11, the on-chip Power-On Reset feature is being used (MCLR and VDD are tied together). The VDD is stable before the start-up timer times out and there is no problem in getting a proper reset. However, Figure 7-12 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses a high on the MCLR/VPP pin, and when the MCLR/VPP pin (and VDD) actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 7-9).

Note: When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be meet to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

For more information on PIC16C5X POR, see *Power-Up Considerations* - AN522 in the <u>Embedded</u> <u>Control Handbook</u>.

The POR circuit does not produce an internal reset when VDD declines.

FIGURE 7-9: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



• R1 = 100Ω to 1 k Ω will limit any current flowing into \overline{MCLR} from external capacitor C in the event of \overline{MCLR} pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).



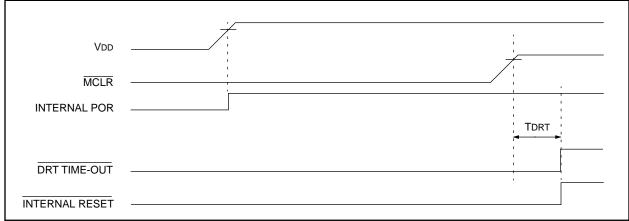


FIGURE 7-11: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): FAST VDD RISE TIME

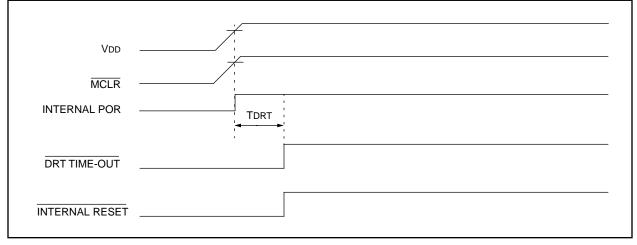
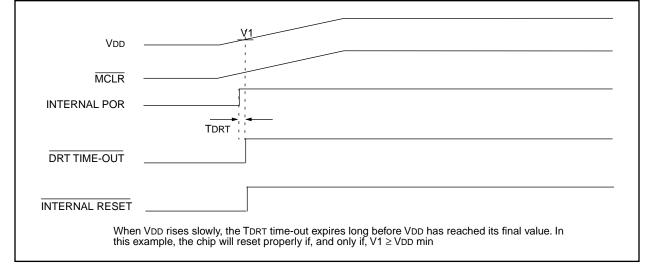


FIGURE 7-12: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): SLOW VDD RISE TIME



7.5 Device Reset Timer (DRT)

The Device Reset Timer (DRT) provides a fixed 18 ms nominal time-out on reset. The DRT operates on an internal RC oscillator. The processor is kept in RESET as long as the DRT is active. The DRT delay allows VDD to rise above VDD min., and for the oscillator to stabilize.

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the device in a RESET condition for approximately 18 ms after the voltage on the MCLR/VPP pin has reached a logic high (VIH) level. Thus, external RC networks connected to the MCLR input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.

The Device Reset time delay will vary from chip to chip due to VDD, temperature, and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out. This is particularly important for applications using the WDT to wake the PIC16C5X from SLEEP mode automatically.

7.6 <u>Watchdog Timer (WDT) (not</u> implemented on PIC16C52)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins have been stopped, for example, by execution of a SLEEP instruction. During normal operation or SLEEP, a WDT reset or wake-up reset generates a device RESET.

The $\overline{\text{TO}}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer reset.

The WDT can be permanently disabled by programming the configuration bit WDTE as a '0' (Section 7.1). Refer to the PIC16C5X Programming Specifications (Literature Number DS30190) to determine how to access the configuration word.

7.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, time-out a period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see DC specs).

Under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

7.6.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The SLEEP instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT wake-up reset.

FIGURE 7-13: WATCHDOG TIMER BLOCK DIAGRAM

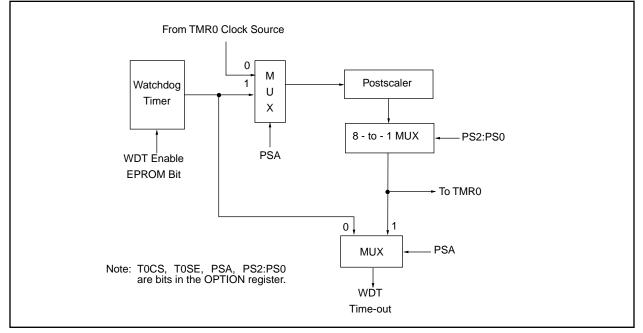


TABLE 7-5: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on MCLR and WDT Reset
N/A	OPTION	_		TOCS	T0SE	PSA	PS2	PS1	PS0	11 1111	11 1111

Legend: Shaded boxes = Not used by Watchdog Timer,

- = unimplemented, read as '0', u = unchanged

7.7 <u>Time-Out Sequence and Power Down</u> Status Bits (TO/PD)

The \overline{TO} and \overline{PD} bits in the STATUS register can be tested to determine if a RESET condition has been caused by a power-up condition, a \overline{MCLR} or Watchdog Timer (WDT) reset, or a \overline{MCLR} or WDT wake-up reset.

TABLE 7-6:TO/PD STATUS AFTER
RESET

ТО	PD	RESET was caused by
1	1	Power-up (POR)
u	u	MCLR reset (normal operation) ⁽¹⁾
1	0	MCLR wake-up reset (from SLEEP)
0	1	WDT reset (normal operation)
0	0	WDT wake-up reset (from SLEEP)

Legend: u = unchanged

Note 1: The TO and PD bits maintain their status (u) until a reset occurs. A low-pulse on the MCLR input does not change the TO and PD status bits.

These STATUS bits are only affected by events listed in Table 7-7.

TABLE 7-7:EVENTS AFFECTING TO/PDSTATUS BITS

Event	TO	PD	Remarks
Power-up	1	1	
WDT Time-out	0	u	No effect on PD
SLEEP instruction	1	0	
CLRWDT instruction	1	1	

Legend: u = unchanged

A WDT time-out will occur regardless of the status of the $\overline{\text{TO}}$ bit. A SLEEP instruction will be executed, regardless of the status of the $\overline{\text{PD}}$ bit. Table 7-6 reflects the status of $\overline{\text{TO}}$ and $\overline{\text{PD}}$ after the corresponding event.

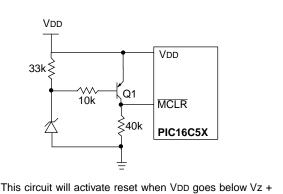
Table 7-3 lists the reset conditions for the special function registers, while Table 7-4 lists the reset conditions for all the registers.

7.8 Reset on Brown-Out

A brown-out is a condition where device power (VDD) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

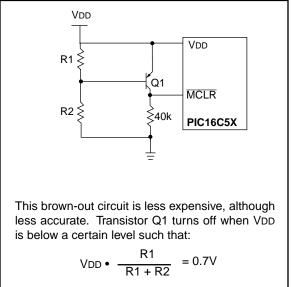
To reset PIC16C5X devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 7-14 and Figure 7-15.

FIGURE 7-14: BROWN-OUT PROTECTION CIRCUIT 1



This circuit will activate reset when VDD goes below Vz + 0.7V (where Vz = Zener voltage).

FIGURE 7-15: BROWN-OUT PROTECTION CIRCUIT 2



7.9 Power-Down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

7.9.1 SLEEP

The Power-Down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the \overline{TO} bit (STATUS<4>) is set, the \overline{PD} bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low, or hi-impedance).

It should be noted that a RESET generated by a WDT time-out does not drive the $\overline{\text{MCLR}}/\text{VPP}$ pin low.

For lowest current consumption while powered down, the T0CKI input should be at VDD or Vss and the $\overline{\text{MCLR}}/\text{VPP}$ pin must be at a logic high level (VIH $\overline{\text{MCLR}}$).

7.9.2 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

- 1. An external reset input on MCLR/VPP pin.
- 2. A Watchdog Timer time-out reset (if WDT was enabled).

Both of these events cause a device reset. The \overline{TO} and \overline{PD} bits can be used to determine the cause of device reset. The \overline{TO} bit is cleared if a WDT time-out occurred (and caused wake-up). The \overline{PD} bit, which is set on power-up, is cleared when SLEEP is invoked.

The WDT is cleared when the device wakes from sleep, regardless of the wake-up source.

7.10 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note: Microchip does not recommend code protecting windowed devices.

7.11 ID Locations (not implemented on PIC16C52)

Four memory locations are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '1's.

Note: Microchip will assign a unique pattern number for QTP and SQTP requests and for ROM devices. This pattern number will be unique and traceable to the submitted code.

8.0 INSTRUCTION SET SUMMARY

Each PIC16C5X instruction is a 12-bit word divided into an OPCODE, which specifies the instruction type, and one or more operands which further specify the operation of the instruction. The PIC16C5X instruction set summary in Table 8-2 groups the instructions into byte-oriented, bit-oriented, and literal and control operations. Table 8-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator is used to specify which one of the 32 file registers is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

TABLE 8-1:OPCODE FIELD
DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with $x = 0$. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0 (store result in W) d = 1 (store result in file register 'f') Default is $d = 1$
label	Label name
TOS	Top of Stack
PC	Program Counter
WDT	Watchdog Timer Counter
TO	Time-Out bit
PD	Power-Down bit
dest	Destination, either the W register or the specified register file location
[]	Options
()	Contents
\rightarrow	Assigned to
< >	Register bit field
∈	In the set of
italics	User defined term (font is courier)

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μ s. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μ s.

Figure 8-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

FIGURE 8-1: GENERAL FORMAT FOR INSTRUCTIONS

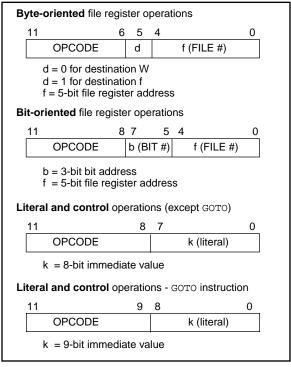


TABLE 8-2: INSTRUCTION SET SUMMARY

Mnemonic,				12-	Bit Opc	ode	Status	
Operan		Description	Cycles	MSb		LSb	Affected	Notes
ADDWF	f,d	Add W and f	1	0001	11df	ffff	C,DC,Z	1,2,4
ANDWF	f,d	AND W with f	1	0001	01df	ffff	Z	2,4
CLRF	f	Clear f	1	0000	011f	ffff	Z	4
CLRW	_	Clear W	1	0000	0100	0000	Z	
COMF	f, d	Complement f	1	0010	01df	ffff	Z	
DECF	f, d	Decrement f	1	0000	11df	ffff	Z	2,4
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	0010	11df	ffff	None	2,4
INCF	f, d	Increment f	1	0010	10df	ffff	Z	2,4
INCFSZ	f, d	Increment f, Skip if 0	1(2)	0011	11df	ffff	None	2,4
IORWF	f, d	Inclusive OR W with f	1	0001	00df	ffff	Z	2,4
MOVF	f, d	Move f	1	0010	00df	ffff	Z	2,4
MOVWF	f	Move W to f	1	0000	001f	ffff	None	1,4
NOP	-	No Operation	1	0000	0000	0000	None	
RLF	f, d	Rotate left f through Carry	1	0011	01df	ffff	С	2,4
RRF	f, d	Rotate right f through Carry	1	0011	00df	ffff	С	2,4
SUBWF	f, d	Subtract W from f	1	0000	10df	ffff	C,DC,Z	1,2,4
SWAPF	f, d	Swap f	1	0011	10df	ffff	None	2,4
XORWF	f, d	Exclusive OR W with f	1	0001	10df	ffff	Z	2,4
BIT-ORIEN	TED FIL	E REGISTER OPERATIONS						
BCF	f, b	Bit Clear f	1	0100	bbbf	ffff	None	2,4
BSF	f, b	Bit Set f	1	0101	bbbf	ffff	None	2,4
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	0110	bbbf	ffff	None	
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	0111	bbbf	ffff	None	
LITERAL A	ND COM	NTROL OPERATIONS						
ANDLW	k	AND literal with W	1	1110	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	1001	kkkk	kkkk	None	1
CLRWDT	k	Clear Watchdog Timer	1	0000	0000	0100	TO, PD	
GOTO	k	Unconditional branch	2	101k	kkkk	kkkk	None	
IORLW	k	Inclusive OR Literal with W	1	1101	kkkk	kkkk	Z	
MOVLW	k	Move Literal to W	1	1100	kkkk	kkkk	None	
OPTION	k	Load OPTION register	1	0000	0000	0010	None	
RETLW	k	Return, place Literal in W	2	1000	kkkk	kkkk	None	
SLEEP	_	Go into standby mode	1	0000	0000	0011	TO, PD	
TRIS	f	Load TRIS register	1	0000	0000	Offf	None	3
XORLW	k	Exclusive OR Literal to W	1	1111	kkkk	kkkk	Z	

Note 1: The 9th bit of the program counter will be forced to a '0' by any instruction that writes to the PC except for GOTO. (See individual device data sheets, Memory Section/Indirect Data Addressing, INDF and FSR Registers)

2: When an I/O register is modified as a function of itself (e.g. MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

3: The instruction TRIS f, where f = 5 or 6 causes the contents of the W register to be written to the tristate latches of PORTA or B respectively. A '1' forces the pin to a hi-impedance state and disables the output buffers.

4: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared (if assigned to TMR0).

ADDWF	Add W and f
Syntax:	[<i>label</i>] ADDWF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in \ [0,1] \end{array}$
Operation:	(W) + (f) \rightarrow (dest)
Status Affected:	C, DC, Z
Encoding:	0001 11df ffff
Description:	Add the contents of the W register and register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example:	ADDWF FSR, 0
Before Instru W = FSR = After Instruct W = FSR =	0x17 0xC2 ion 0xD9

ANDWF	AND W with f				
Syntax:	[label] ANDWF f,d				
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in \ [0,1] \end{array}$				
Operation:	(W) .AND. (f) \rightarrow (dest)				
Status Affected:	Z				
Encoding:	0001 01df ffff				
Description:	The contents of the W register are AND'ed with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.				
Words:	1				
Cycles:	1				
Example:	ANDWF FSR, 1				
Before Instru W = FSR =	0x17				
After Instruc W = FSR =	0x17				

ANDLW	And liter	al with W	/	
Syntax:	[<i>label</i>] ANDLW k			
Operands:	$0 \le k \le 255$			
Operation:	(W).AND. (k) \rightarrow (W)			
Status Affected:	Z			
Encoding:	1110	kkkk	kkkk	
Description:	The conter AND'ed wi result is pla	th the eigh	nt-bit literal	'k'. The
Words:	1			
Cycles:	1			
Example:	ANDLW	0x5F		
Before Instru	ction			
W =	0xA3			
After Instruct W =	ion 0x03			

BCF	Bit Clear	f		
Syntax:	[label] BCF f,b			
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ 0 \leq b \leq 7 \end{array}$			
Operation:	$0 \rightarrow (f < b >)$			
Status Affected:	None			
Encoding:	0100	bbbf	ffff	
Description:	Bit 'b' in re	gister 'f' is	cleared.	I
Words:	1			
Cycles:	1			
Example:	BCF	FLAG_REG	B, 7	
Before Instruction FLAG_REG = 0xC7				
After Instruct FLAG_R	tion EG = 0x47	,		

BSF	Bit Set f				
Syntax:	[label] BSF f,b				
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ 0 \leq b \leq 7 \end{array}$				
Operation:	$1 \rightarrow (f < b >)$				
Status Affected:	None				
Encoding:	0101	bbbf	ffff		
Description:	Bit 'b' in re	gister 'f' is	set.		
Words:	1				
Cycles:	1				
Example:	BSF	FLAG_REG	G, 7		
Before Instruction FLAG_REG = 0x0A					
After Instruction FLAG_REG = 0x8A					

BTFSC	Bit Test	f, Skip if	Clear	
Syntax:	[label]	BTFSC	f,b	
Operands:	$0 \le f \le 3$ $0 \le b \le 3$			
Operation:	skip if (f) = 0		
Status Affected:	None			
Encoding:	0110	bbbf	ffff	
Description:		n register 'f n is skippe		he next
	fetched c execution	s 0 then the luring the c is discard linstead, m on.	urrent instr ed, and an	uction NOP is
Words:	1			
Cycles:	1(2)			
Example:	HERE FALSE TRUE	BTFSC GOTO •	FLAG,1 PROCESS	_CODE
Before Instru	uction			
PC	=	address	(HERE)	
After Instruc if FLAG< PC if FLAG< PC	1> = =	0, address(1, address(1		

BTFSS	Bit Test f, Skip if Set
Syntax:	[label] BTFSS f,b
Operands:	$0 \le f \le 31$ $0 \le b < 7$
Operation:	skip if (f) = 1
Status Affected:	None
Encoding:	0111 bbbf ffff
Description:	If bit 'b' in register 'f' is '1' then the next instruction is skipped. If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and an NOP is executed instead, making this a 2 cycle instruction.
Words:	1
Cycles:	1(2)
Example:	HERE BTFSS FLAG,1 FALSE GOTO PROCESS_CODE TRUE • •
Before Instru PC	address (HERE)
After Instruc If FLAG< PC if FLAG< PC	<pre>1> = 0, = address (FALSE);</pre>

CALL	Subroutine Call
Syntax:	[<i>label</i>] CALL k
Operands:	$0 \le k \le 255$
Operation:	$\begin{array}{l} (PC) + 1 \rightarrow Top \text{ of Stack}; \\ k \rightarrow PC < \!\!7:0\!\!>; \\ (STATUS < \!\!6:5\!\!>) \rightarrow PC < \!\!10:9\!\!>; \\ 0 \rightarrow PC < \!\!8\!\!> \end{array}$
Status Affected:	None
Encoding:	1001 kkkk kkkk
Description:	Subroutine call. First, return address (PC+1) is pushed onto the stack. The eight bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STA- TUS<6:5>, PC<8> is cleared. CALL is a two cycle instruction.
Words:	1
Cycles:	2
Example:	HERE CALL THERE
Before Instru PC =	ction address (HERE)
	ion address (THERE) address (HERE + 1)

CLRF	Clear f		
Syntax:	[label]	CLRF f	
Operands:	$0 \le f \le 31$	l	
Operation:	$\begin{array}{c} 00h \rightarrow (f) \\ 1 \rightarrow Z \end{array}$);	
Status Affected:	Z		
Encoding:	0000	011f	ffff
Description:	The conte and the Z	•	ster 'f' are cleared
Words:	1		
Cycles:	1		
Example:	CLRF	FLAG_REG	5
Before Instru FLAG_RI		0x5A	
After Instruct FLAG_RI Z		0x00 1	

CLRW	Clear W
Syntax:	[label] CLRW
Operands:	None
Operation:	$\begin{array}{l} 00h \rightarrow (W); \\ 1 \rightarrow Z \end{array}$
Status Affected:	Z
Encoding:	0000 0100 0000
Description:	The W register is cleared. Zero bit (Z) is set.
Words:	1
Cycles:	1
Example:	CLRW
Before Instru W =	uction 0x5A
After Instruc	
W = Z =	0x00 1
_	
CLRWDT	Clear Watchdog Timer
Syntax:	[label] CLRWDT
Operands:	None
Operation:	00h → WDT; 0 → WDT prescaler (if assigned); 1 → $\overline{\text{TO}}$;
Status Affected:	$1 \rightarrow \overline{PD}$ TO, \overline{PD}
Encoding:	0000 0000 0100
Description:	The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits TO and PD are set.
Words:	1
Cycles:	1
Example:	CLRWDT
Before Instru WDT cou	
After Instruc WDT cou WDT pre TO PD	unter = 0x00

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COMF	Complement f
Syntax:	[label] COMF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in \left[0,1 \right] \end{array}$
Operation:	$(\overline{f}) \rightarrow (dest)$
Status Affected:	Z
Encoding:	0010 01df ffff
Description:	The contents of register 'f' are comple- mented. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example:	COMF REG1,0
Before Instru REG1	uction = 0x13
After Instruc REG1 W	tion = 0x13 = 0xEC

DECF	Decrement f
Syntax:	[label] DECF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in \ [0,1] \end{array}$
Operation:	$(f) - 1 \rightarrow (dest)$
Status Affected:	Z
Encoding:	0000 11df ffff
Description:	Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example:	decf cnt, 1
Before Instru CNT Z After Instruct	= 0x01 = 0
CNT Z	= 0x00 = 1

	Degrament & Chin if 0
DECFSZ	Decrement f, Skip if 0
Syntax:	[<i>label</i>] DECFSZ f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in \left[0,1\right] \end{array}$
Operation:	(f) $- 1 \rightarrow d$; skip if result = 0
Status Affected:	None
Encoding:	0010 11df ffff
Description:	The contents of register 'f' are decre- mented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
	If the result is 0, the next instruction, which is already fetched, is discarded and an NOP is executed instead mak- ing it a two cycle instruction.
Words:	1
Cycles:	1(2)
Example:	HERE DECFSZ CNT, 1 GOTO LOOP
	CONTINUE •
	•
Before Instru	iction
PC	= address (HERE)
After Instruct CNT if CNT PC if CNT PC	tion = CNT - 1; = 0, = address (CONTINUE); ≠ 0, = address (HERE+1)

GOTO	Unconditional Branch
Syntax:	[<i>label</i>] GOTO k
Operands:	$0 \le k \le 511$
Operation:	$k \rightarrow PC < 8:0>;$ STATUS < 6:5> $\rightarrow PC < 10:9>$
Status Affected:	None
Encoding:	101k kkkk kkkk
Description:	GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The upper bits of PC are loaded from STATUS<6:5>. GOTO is a two cycle instruction.
Words:	1
Cycles:	2
Example:	GOTO THERE
After Instruc PC =	tion address (THERE)

INCF	Increme	nt f		
Syntax:	[label]	INCF f,	d	
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in \ [0,1] \end{array}$			
Operation:	(f) + 1 \rightarrow	(dest)		
Status Affected:	Z			
Encoding:	0010	10df	ffff	
Description:	The conte mented. If the W regi placed bac	'd' is 0 the	result is p s 1 the res	laced in
Words:	1			
Cycles:	1			
Example:	INCF	CNT,	1	
Before Instru CNT Z After Instruct CNT Z	= 0xFF = 0			

INCFSZ	Increment f, Skip if 0
Syntax:	[label] INCFSZ f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in \left[0,1\right] \end{array}$
Operation:	(f) + 1 \rightarrow (dest), skip if result = 0
Status Affected:	None
Encoding:	0011 11df ffff
Description:	The contents of register 'f' are incre- mented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. If the result is 0, then the next instruc- tion, which is already fetched, is dis- carded and an NOP is executed instead making it a two cycle instruc- tion.
Words:	1
Cycles:	1(2)
Example:	HERE INCFSZ CNT, 1 GOTO LOOP CONTINUE • •
Before Instru	iction
PC	= address (HERE)
After Instruct CNT if CNT PC if CNT PC	tion = CNT + 1; = 0, = address (CONTINUE); ≠ 0, = address (HERE +1)

	Inclusive OR literal with W
Syntax:	[<i>label</i>] IORLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .OR. (k) \rightarrow (W)
Status Affected:	Z
Encoding:	1101 kkkk kkkk
Description:	The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W register.
Words:	1
Cycles:	1
Example:	IORLW 0x35
Before Instru W =	0x9A
After Instruct W = Z =	ion 0xBF 0
IORWF	Inclusive OR W with f
Syntax:	
Oymax.	[label] IORWF f,d
Operands:	[label] lock VF i,d $0 \le f \le 31$ $d \in [0,1]$
-	$0 \le f \le 31$
Operands:	$0 \le f \le 31$ $d \in [0,1]$
Operands: Operation:	$0 \le f \le 31$ d \equiv [0,1] (W).OR. (f) \rightarrow (dest)
Operands: Operation: Status Affected:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \\ (W).OR. (f) \rightarrow (dest) \\ Z \end{array}$
Operands: Operation: Status Affected: Encoding:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \\ (W).OR. (f) \rightarrow (dest) \\ Z \\ \hline \hline 0001 00df ffff \\ Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is \\ \end{array}$
Operands: Operation: Status Affected: Encoding: Description:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \\ (W).OR. (f) \rightarrow (dest) \\ Z \\ \hline \hline 0001 00df ffff \\ Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. \\ \end{array}$
Operands: Operation: Status Affected: Encoding: Description: Words:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \\ (W).OR. (f) \rightarrow (dest) \end{array}$ Z $\begin{array}{c} \hline 0001 00df ffff \\ \hline \\ Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. 1 \\ 1 \end{array}$
Operands: Operation: Status Affected: Encoding: Description: Words: Cycles:	$\begin{array}{llllllllllllllllllllllllllllllllllll$

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MOVF	Move f			
Syntax:	[label]	MOVF	f,d	
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in \ [0,1] \end{array}$			
Operation:	(f) \rightarrow (de	st)		
Status Affected:	Z			
Encoding:	0010	00df	ffff	
Description:	The conte destination the W regi is file regis a file regis affected.	n 'd'. If 'd' is ster. If 'd' is ster 'f'. 'd' is	s 0, destina s 1, the dea s 1 is usefu	ation is stination ul to test
Words:	1			
Cycles:	1			
Example:	MOVF	FSR,	0	
After Instruc	tion			
W =	value in F	SR registe	r	

MOVWF	Move W	to f		
Syntax:	[label]	MOVWF	f	
Operands:	$0 \le f \le 31$			
Operation:	$(W) \rightarrow (f)$)		
Status Affected:	None			
Encoding:	0000	001f	ffff	
Description:	Move data ter 'f'.	from the	N register	to regis-
Words:	1			
Cycles:	1			
Example:	MOVWF	TEMP_REC	3	
Before Instru TEMP_R W	EG =	0xFF 0x4F		
After Instruct TEMP_R W	EG =	0x4F 0x4F		

MOVLW Move Literal to W Syntax: [label] MOVLW k Operands: $0 \leq k \leq 255$ Operation: $\mathsf{k}\to(\mathsf{W})$ Status Affected: None 1100 Encoding: kkkk kkkk The eight bit literal 'k' is loaded into the Description: W register. The don't cares will assemble as 0s. Words: 1 Cycles: 1 Example: MOVLW 0x5A After Instruction W 0x5A =

NOP	No Oper	ation	
Syntax:	[label]	NOP	
Operands:	None		
Operation:	No opera	ation	
Status Affected:	None		
Encoding:	0000	0000	0000
Description:	No opera	ation.	•
Words:	1		
Cycles:	1		
Example:	NOP		

OPTION	Load OF	TION Re	gister	
Syntax:	[label]	OPTION	1	
Operands:	None			
Operation:	$(W)\toO$	PTION		
Status Affected:	None			
Encoding:	0000	0000	0010	
Description:		ent of the W PTION reg	0	s loaded
Words:	1			
Cycles:	1			
Example	OPTION			
Before Instru W	iction = 0x07			
After Instruct OPTION				

RETLW	Return with	Literal in W
Syntax:	[label] RE	TLW k
Operands:	$0 \le k \le 255$	
Operation:	$\begin{array}{l} k \rightarrow (W);\\ TOS \rightarrow PC \end{array}$	
Status Affected:	None	
Encoding:	1000 kk	kk kkkk
Description:	bit literal 'k'. The loaded from the	r is loaded with the eight ne program counter is ne top of the stack (the s). This is a two cycle
Words:	1	
Cycles:	2	
Example:	CALL TABLE	;W contains
·		;table offset
	_	;value. ;W now has table
		;w now nas table ;value.
	•	, varaet
TABLE	ADDWF PC	;W = offset
	RETLW kl	;Begin table
	RETLW k2	i
	•	
	•	
	RETLW kn	; End of table
Before Instru	uction	
W =	0x07	
After Instruct	tion	
W =	value of k8	

RLF	Rotate Left f through Carry
Syntax:	[<i>label</i>] RLF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in \left[0,1\right] \end{array}$
Operation:	See description below
Status Affected:	С
Encoding:	0011 01df ffff
Description:	The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.
Words:	1
Cycles:	1
Example:	RLF REG1,0
Before Instru	iction
REG1 C	= 1110 0110 = 0
After Instruct	J. J
REG1	= 1110 0110
W	= 1100 1100
С	= 1
RRF	Rotate Right f through Carry
RRF	Rotate Right f through Carry
Syntax:	[label] RRF f,d
Syntax:	[<i>label</i>] RRF f,d $0 \le f \le 31$
Syntax: Operands:	$\begin{bmatrix} label \end{bmatrix} RRF f,d$ $0 \le f \le 31$ $d \in [0,1]$
Syntax: Operands: Operation:	[<i>label</i>] RRF f,d $0 \le f \le 31$ $d \in [0,1]$ See description below
Syntax: Operands: Operation: Status Affected:	$\begin{bmatrix} label \end{bmatrix} RRF f,d$ $0 \le f \le 31$ $d \in [0,1]$ See description below C $0011 00df ffff$ The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the
Syntax: Operands: Operation: Status Affected: Encoding:	$\begin{bmatrix} label \end{bmatrix} RRF f,d$ $0 \le f \le 31$ $d \in [0,1]$ See description below C $0011 00df ffff$ The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
Syntax: Operands: Operation: Status Affected: Encoding: Description:	$[label] RRF f,d$ $0 \le f \le 31$ $d \in [0,1]$ See description below C $0011 00df ffff$ The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed in the back in register 'f'. $C = C = C = C = C$
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words:	[<i>label</i>] RRF f,d $0 \le f \le 31$ $d \in [0,1]$ See description below C 0011 00df ffff The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f' C register 'f' 1
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles:	[<i>label</i>] RRF f,d $0 \le f \le 31$ $d \in [0,1]$ See description below C 0011 00df ffff The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. C register 'f' 1 1 RRF REG1, 0
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example:	[<i>label</i>] RRF f,d $0 \le f \le 31$ $d \in [0,1]$ See description below C 0011 00df ffff The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. C register 'f' 1 1 RRF REG1, 0
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example: Before Instru REG1 C After Instruct	[<i>label</i>] RRF f,d $0 \le f \le 31$ $d \in [0,1]$ See description below C 0011 00df ffff The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. C register 'f' 1 1 RRF REG1, 0 iction = 1110 0110 = 0
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example: Before Instru REG1 C	[<i>label</i>] RRF f,d $0 \le f \le 31$ $d \in [0,1]$ See description below C 0011 00df ffff The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. C register 'f' 1 1 RRF REG1, 0 iction = 1110 0110 = 0

SLEEP	Enter SLEEP Mode	SUBWF	Subtract W from f
Syntax:	[label] SLEEP	Syntax:	[<i>label</i>] SUBWF f,d
Operands: Operation:	None $00h \rightarrow WDT;$	Operands:	$\begin{array}{l} 0 \leq f \leq 31 \\ d \in [0,1] \end{array}$
operation.	$0 \rightarrow WDT$ prescaler;	Operation:	$(f) - (W) \rightarrow (dest)$
	$1 \rightarrow \overline{\text{TO}};$	Status Affected:	C, DC, Z
	$0 \rightarrow \overline{PD}$	Encoding:	0000 10df ffff
Status Affected: Encoding: Description:	TO, PD 0000 0001 Time-out status bit (TO) is set. The power down status bit (PD) is cleared.	Description:	Subtract (2's complement method) the W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.
	The WDT and its prescaler are	Words:	1
	cleared. The processor is put into SLEEP mode	Cycles:	1
	with the oscillator stopped. See sec-	Example 1:	SUBWF REG1, 1
Words: Cycles: Example:	tion on SLEEP for more details. 1 1 SLEEP	Before Instr REG1 W C After Instruct REG1 W C <u>Example 2</u> : Before Instr REG1 W C After Instruct REG1 W	= 3 = 2 = ? ction = 1 = 2 = 1 ; result is positive ruction = 2 = 2 = ? ction = 0 = 2
		C <u>Example 3</u> : Before Instr REG1 W C	= 1 ; result is zero uction = 1 = 2 = ?
		After Instruc REG1 W C	

SWAPF	Swap Ni	bbles in	f	
Syntax:	[label]	SWAPF	f,d	
Operands:	$0 \le f \le 3^{2}$ $d \in [0,1]$	1		
Operation:	· ,	ightarrow (dest< $ ightarrow$) $ ightarrow$ (dest<		
Status Affected:	None			
Encoding:	0011	10df	ffff	
Description:	'f' are excl placed in '	nanged. If	nibbles of 'd' is 0 the If 'd' is 1 th 'f'.	result is
Words:	1			
Cycles:	1			
Example	SWAPF	REG1,	0	
Before Instru REG1	uction = 0xA5	5		
After Instruc REG1 W	tion = 0xA5 = 0X54			

TRIS	Load TRIS Register
Syntax:	[<i>label</i>] TRIS f
Operands:	f = 5, 6 or 7
Operation:	(W) \rightarrow TRIS register f
Status Affected:	None
Encoding:	0000 0000 0fff
Description:	TRIS register 'f' (f = 5, 6, or 7) is loaded with the contents of the W register
Words:	1
Cycles:	1
Example	TRIS PORTA
Before Instru W	iction = 0XA5
After Instruct TRISA	0, 0, 0

XORLW	Exclusive OR literal with W
Syntax:	[<i>label</i>] XORLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .XOR. $k \rightarrow (W)$
Status Affected:	Z
Encoding:	1111 kkkk kkkk
Description:	The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.
Words:	1
Cycles:	1
Example:	XORLW 0xAF
Before Instru W =	uction 0xB5
After Instruc W =	tion 0x1A
XORWF	
	Exclusive OR W with f
Syntax:	[label] XORWF f,d
Syntax:	[<i>label</i>] XORWF f,d $0 \le f \le 31$
Syntax: Operands:	$\begin{bmatrix} label \end{bmatrix} \text{ XORWF} f,d$ $0 \le f \le 31$ $d \in [0,1]$
Syntax: Operands: Operation:	$\begin{bmatrix} label \end{bmatrix} \text{ XORWF} f,d$ $0 \le f \le 31$ $d \in [0,1]$ (W) .XOR. (f) \rightarrow (dest)
Syntax: Operands: Operation: Status Affected:	$\begin{bmatrix} label \end{bmatrix} \text{ XORWF} f,d$ $0 \le f \le 31$ $d \in [0,1]$ (W) .XOR. (f) \rightarrow (dest) Z
Syntax: Operands: Operation: Status Affected: Encoding:	$\begin{bmatrix} label \end{bmatrix} \text{ XORWF } f,d$ $0 \le f \le 31$ $d \in [0,1]$ (W) .XOR. (f) \rightarrow (dest) Z $\boxed{0001 10df ffff}$ Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is
Syntax: Operands: Operation: Status Affected: Encoding: Description:	$\begin{bmatrix} label \end{bmatrix} \text{ XORWF } f,d$ $0 \le f \le 31$ $d \in [0,1]$ (W) .XOR. (f) \rightarrow (dest) Z $\boxed{0001 10df ffff}$ Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words:	$\begin{bmatrix} label \end{bmatrix} \text{ XORWF } f,d$ $0 \le f \le 31$ $d \in [0,1]$ $(W) . \text{XOR. } (f) \rightarrow (\text{dest})$ Z $\boxed{0001 10df ffff}$ Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'. 1
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles:	[<i>label</i>] XORWF f,d $0 \le f \le 31$ $d \in [0,1]$ (W) .XOR. (f) \rightarrow (dest) Z $\boxed{0001 10df ffff}$ Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'. 1 1 XORWF REG, 1
Syntax: Operands: Operation: Status Affected: Encoding: Description: Words: Cycles: Example Before Instruction	$\begin{bmatrix} label \end{bmatrix} \text{ XORWF } f,d \\ 0 \le f \le 31 \\ d \in [0,1] \\ (W) . \text{XOR. } (f) \rightarrow (\text{dest}) \\ Z \\ \hline 0001 & 10df & \text{ffff} \\ Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'. 1 \\ 1 \\ 1 \\ \text{XORWF } REG, 1 \\ \text{Juction} \\ = 0xAF \\ = 0xB5 \\ \end{bmatrix}$

NOTES:

9.0 DEVELOPMENT SUPPORT

9.1 <u>Development Tools</u>

The PIC16/17 microcontrollers are supported with a full range of hardware and software development tools:

- PICMASTER/PICMASTER CE Real-Time In-Circuit Emulator
- ICEPIC Low-Cost PIC16C5X and PIC16CXXX In-Circuit Emulator
- PRO MATE[®] II Universal Programmer
- PICSTART[®] Plus Entry-Level Prototype Programmer
- PICDEM-1 Low-Cost Demonstration Board
- PICDEM-2 Low-Cost Demonstration Board
- PICDEM-3 Low-Cost Demonstration Board
- MPASM Assembler
- MPLAB[™] SIM Software Simulator
- MPLAB-C (C Compiler)
- Fuzzy Logic Development System (*fuzzy*TECH[®]–MP)

9.2 <u>PICMASTER: High Performance</u> <u>Universal In-Circuit Emulator with</u> <u>MPLAB IDE</u>

The PICMASTER Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for all microcontrollers in the PIC12C5XX, PIC14C000, PIC16C5X, PIC16C5XX and PIC17CXX families. PICMASTER is supplied with the MPLAB[™] Integrated Development Environment (IDE), which allows editing, "make" and download, and source debugging from a single environment.

Interchangeable target probes allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the PICMASTER allows expansion to support all new Microchip microcontrollers.

The PICMASTER Emulator System has been designed as a real-time emulation system with advanced features that are generally found on more expensive development tools. The PC compatible 386 (and higher) machine platform and Microsoft Windows[®] 3.x environment were chosen to best make these features available to you, the end user.

A CE compliant version of PICMASTER is available for European Union (EU) countries.

9.3 ICEPIC: Low-Cost PIC16CXXX In-Circuit Emulator

ICEPIC is a low-cost in-circuit emulator solution for the Microchip PIC16C5X and PIC16CXXX families of 8-bit OTP microcontrollers.

ICEPIC is designed to operate on PC-compatible machines ranging from 286-AT[®] through Pentium[™] based machines under Windows 3.x environment. ICEPIC features real time, non-intrusive emulation.

9.4 PRO MATE II: Universal Programmer

The PRO MATE II Universal Programmer is a full-featured programmer capable of operating in stand-alone mode as well as PC-hosted mode.

The PRO MATE II has programmable VDD and VPP supplies which allows it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In standalone mode the PRO MATE II can read, verify or program PIC16C5X, PIC16CXXX, PIC17CXX and PIC14000 devices. It can also set configuration and code-protect bits in this mode.

9.5 <u>PICSTART Plus Entry Level</u> <u>Development System</u>

The PICSTART programmer is an easy-to-use, lowcost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. PICSTART Plus is not recommended for production programming.

PICSTART Plus supports all PIC12C5XX, PIC14000, PIC16C5X, PIC16CXXX and PIC17CXX devices with up to 40 pins. Larger pin count devices such as the PIC16C923 and PIC16C924 may be supported with an adapter socket.

9.6 <u>PICDEM-1 Low-Cost PIC16/17</u> <u>Demonstration Board</u>

The PICDEM-1 is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The users can program the sample microcontrollers provided with the PICDEM-1 board, on a PRO MATE II or PICSTART-Plus programmer, and easily test firmware. The user can also connect the PICDEM-1 board to the PICMASTER emulator and download the firmware to the emulator for testing. Additional prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push-button switches and eight LEDs connected to PORTB.

9.7 <u>PICDEM-2 Low-Cost PIC16CXX</u> Demonstration Board

The PICDEM-2 is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-2 board, on a PRO MATE II programmer or PICSTART-Plus, and easily test firmware. The PICMASTER emulator may also be used with the PICDEM-2 board to test firmware. Additional prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push-button switches, a potentiometer for simulated analog input, a Serial EEPROM to demonstrate usage of the I²C bus and separate headers for connection to an LCD module and a keypad.

9.8 PICDEM-3 Low-Cost PIC16CXXX Demonstration Board

The PICDEM-3 is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with a LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-3 board, on a PRO MATE II programmer or PICSTART Plus with an adapter socket, and easily test firmware. The PICMASTER emulator may also be used with the PICDEM-3 board to test firmware. Additional prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include an RS-232 interface, push-button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM-3 board is an LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM-3 provides an additional RS-232 interface and Windows 3.1 software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

9.9 <u>MPLAB Integrated Development</u> <u>Environment Software</u>

The MPLAB IDE Software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a windows based application which contains:

- A full featured editor
- Three operating modes
 - editor
 - emulator
 - simulator
- A project manager
- Customizable tool bar and key mapping
- A status bar with project information

Extensive on-line help

MPLAB allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC16/17 tools (automatically updates all project information)
- Debug using:
- source files
- absolute listing file
- Transfer data dynamically via DDE (soon to be replaced by OLE)
- Run up to four emulators on the same PC

The ability to use MPLAB with Microchip's simulator allows a consistent platform and the ability to easily switch from the low cost simulator to the full featured emulator with minimal retraining due to development tools.

9.10 Assembler (MPASM)

The MPASM Universal Macro Assembler is a PChosted symbolic assembler. It supports all microcontroller series including the PIC12C5XX, PIC14000, PIC16C5X, PIC16CXXX, and PIC17CXX families.

MPASM offers full featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from PICMASTER, Microchip's Universal Emulator System. MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro assembly capability.
- Produces all the files (Object, Listing, Symbol, and special) required for symbolic debug with Microchip's emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a rich directive language to support programming of the PIC16/17. Directives are helpful in making the development of your assemble source code shorter and more maintainable.

9.11 Software Simulator (MPLAB-SIM)

The MPLAB-SIM Software Simulator allows code development in a PC host environment. It allows the user to simulate the PIC16/17 series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/ output radix can be set by the user and the execution can be performed in; single step, execute until break, or in a trace mode.

MPLAB-SIM fully supports symbolic debugging using MPLAB-C and MPASM. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

9.12 <u>C Compiler (MPLAB-C)</u>

The MPLAB-C Code Development System is a complete 'C' compiler and integrated development environment for Microchip's PIC16/17 family of micro-controllers. The compiler provides powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compiler provides symbol information that is compatible with the MPLAB IDE memory display.

9.13 <u>Fuzzy Logic Development System</u> (*fuzzy*TECH-MP)

*fuzzy*TECH-MP fuzzy logic development tool is available in two versions - a low cost introductory version, MP Explorer, for designers to gain a comprehensive working knowledge of fuzzy logic system design; and a full-featured version, *fuzzy*TECH-MP, edition for implementing more complex systems.

Both versions include Microchip's *fuzzy*LAB[™] demonstration board for hands-on experience with fuzzy logic systems implementation.

9.14 <u>MP-DriveWay™ – Application Code</u> <u>Generator</u>

MP-DriveWay is an easy-to-use Windows-based Application Code Generator. With MP-DriveWay you can visually configure all the peripherals in a PIC16/17 device and, with a click of the mouse, generate all the initialization and many functional code modules in C language. The output is fully compatible with Microchip's MPLAB-C C compiler. The code produced is highly modular and allows easy integration of your own code. MP-DriveWay is intelligent enough to maintain your code through subsequent code generation.

9.15 <u>SEEVAL[®] Evaluation and</u> <u>Programming System</u>

The SEEVAL SEEPROM Designer's Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPROM product including Smart Serials[™] and secure serials. The Total Endurance[™] Disk is included to aid in tradeoff analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

9.16 <u>KEELOQ[®] Evaluation and</u> <u>Programming Tools</u>

KEELOQ evaluation and programming tools support Microchips HCS Secure Data Products. The HCS evaluation kit includes an LCD display to show changing codes, a decoder to decode transmissions, and a programming interface to program test transmitters.

TABLE 9-1: DEVELOPMENT TOOLS FROM MICROCHI
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		PIC12C5XX	PIC14000	PIC16C5X	PIC16CXXX	PIC16C6X	PIC16C7XX	PIC16C8X	PIC16C9XX	PIC17C4X	PIC17C75X	24CXX 25CXX 93CXX	HCS200 HCS300 HCS301
stoubor	PICMASTER®/ PICMASTER-CE In-Circuit Emulator	2	7	7	7	7	7	7	>	>	Available 3Q97		
Emulator P	ICEPIC Low-Cost In-Circuit Emulator	7		7	7	7	7	7					
	MPLAB™ Integrated Development Environment	7	7	7	7	7	7	7	7	7	7		
slo	MPLAB TM C Compiler	7	>	>	7	7	7	7	2	7	>		
oT əıswitoč	<i>fuzz</i> yTECH®-MP Explorer/Edition Fuzzy Logic Dev. Tool	7	7	7	7	7	7	7	7	7			
\$	MP-DriveWay™ Applications Code Generator			7	7	7	7	7		7			
	Total Endurance™ Software Model											7	
	PICSTART® Lite Ultra Low-Cost Dev. Kit			7		7	7	7					
ຌຒຆຨຎ	PICSTART [®] Plus Low-Cost Universal Dev. Kit	7	7	7	7	7	7	7	7	2	7		
Ριοθι	PRO MATE [®] II Universal Programmer	7	7	7	7	7	7	7	7	7	>	7	7
	KEELOQ [®] Programmer												7
	SEEVAL [®] Designers Kit											7	
spie	PICDEM-1			7	7			7		7			
0 B 0	PICDEM-2					7	7						
Dem	PICDEM-3								7				
	KEELOQ [®] Evaluation Kit												7

10.0 ELECTRICAL CHARACTERISTICS - PIC16C52

Absolute Maximum Ratings†

Ambient Temperature under bias	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on VDD with respect to VSS	
Voltage on MCLR with respect to Vss	0 V to +14 V
Voltage on all other pins with respect to Vss	–0.6 V to (VDD + 0.6 V)
Total Power Dissipation ⁽¹⁾	800 mW
Max. Current out of Vss pin	150 mA
Max. Current into Vod pin	50 mA
Max. Current into an input pin (T0CKI only)	±500 μA
Input Clamp Current, Iк (Vi < 0 or Vi > VDD)	±20 mA
Output Clamp Current, Iок (Vo < 0 or Vo > VDD)	±20 mA
Max. Output Current sunk by any I/O pin	10 mA
Max. Output Current sourced by any I/O pin	10 mA
Max. Output Current sourced by a single I/O port (PORTA or B)	10 mA
Max. Output Current sunk by a single I/O port (PORTA or B)	10 mA
Note 1: Power Dissipation is calculated as follows: Pdis = VDD x {IDD $-\Sigma$ IOH} + Σ {(VDD $-V$	OH) X IOH} + Σ (VOL X IOL)

[†]NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

10.1 <u>DC Characteristics:</u> <u>PIC16C52-04 (Commercial)</u> <u>PIC16C52-04I (Industrial)</u>

DC Characteristics Power Supply Pins	$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^\circ C \leq T A \leq +70^\circ C \mbox{ (commercial)} \\ -40^\circ C \leq T A \leq +85^\circ C \mbox{ (industrial)} \end{array}$					
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions
Supply Voltage	Vdd	3.0		6.25	V	Fosc = DC to 4 MHz
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP Mode
Supply Current ^(3,4)	IDD		1.8	3.3	mA	Fosc = 4 MHz, VDD = 5.5 V
Power Down Current ⁽⁵⁾ Commercial Industrial	IPD		0.6 0.6	9 12	μΑ μΑ	VDD = 3.0 V VDD = 3.0 V

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD.

- b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
- 4: For RC option, does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
- 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

10.2 DC Characteristics: PIC16C52-04 (Commercial) PIC16C52-04I (Industrial)

DC Characteristics All Pins Except Power Supply Pins		Operating To	emperatu	re 0°C ≤ –40°C ≤	(unless otherwise specified) TA \leq +70°C (commercial) TA \leq +85°C (industrial) escribed in Section 10.1.			
Characteristic	Sym	Min	Typ ⁽¹⁾	Мах	Units	Conditions		
Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger)	VIL	Vss Vss Vss Vss Vss		0.2 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V V	Pin at hi-impedance RC ⁽⁴⁾ option only XT option		
Input High Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger)	Vih	0.45 VDD 2.0 0.36 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD		VDD VDD VDD VDD VDD VDD VDD	V V V V V V	For all VDD ⁽⁵⁾ 4.0 V < VDD \leq 5.5 V ⁽⁵⁾ VDD > 5.5 V RC ⁽⁴⁾ option only XT option		
Hysteresis of Schmitt Trigger inputs	VHYS	0.15Vdd*			V			
Input Leakage Current ^(2,3) I/O ports MCLR T0CKI OSC1	Ιι∟	-1 -5 -3 -3	0.5 0.5 0.5 0.5	+1 +5 +3 +3	μΑ μΑ μΑ μΑ μΑ	$\label{eq:statestar} \begin{array}{l} \mbox{For VDD} \leq 5.5 \ \mbox{V} \\ \mbox{Vss} \leq \mbox{VpIN} \leq \mbox{Vdd}, \\ \mbox{Pin at hi-impedance} \\ \mbox{VpIN} = \ \mbox{Vss} + 0.25 \ \ \mbox{V} \\ \mbox{VpIN} = \ \mbox{Vdd} \\ \mbox{Vss} \leq \ \mbox{VpIN} \leq \ \mbox{Vdd} \\ \mbox{Vdd} \\ \mbox{Vss} \leq \ \mbox{VpIN} \leq \ \mbox{Vdd} \\ \mbox{Vdd} \\ \mbox{XT option} \end{array}$		
Output Low Voltage I/O ports OSC2/CLKOUT	Vol			0.6 0.6	V V	IOL = 2.0 mA, VDD = 4.5 V IOL = 1.6 mA, VDD = 4.5 V, RC option		
Output High Voltage I/O ports ⁽³⁾ OSC2/CLKOUT	Vон	Vdd – 0.7 Vdd – 0.7			V V	IOH = -2.0 mA, VDD = 4.5 V IOH = -1.0 mA, VDD = 4.5 V, RC option		

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- 2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.
- 3: Negative current is defined as coming out of the pin.
- 4: For RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C52 be driven with external clock in RC mode.
- 5: The user may use the better of the two specifications.

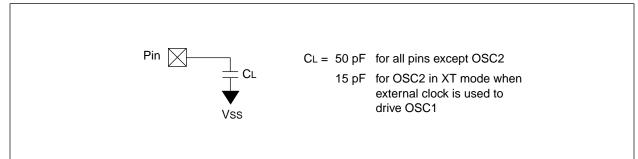
10.3 <u>Timing Parameter Symbology and Load Conditions</u>

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS

2. TppS				
Т				
F	Frequency	Т	Time	
Lowerc	case subscripts (pp) and their meanings	:		
рр				
2	to	mc	MCLR	
ck	CLKOUT	OSC	oscillator	
су	cycle time	os	OSC1	
drt	device reset timer	tO	TOCKI	
io	I/O port			
Upperc	case letters and their meanings:			
S				
F	Fall	P	Period	
н	High	R	Rise	
	Invalid (Hi-impedance)	V	Valid	
L	Low	Z	Hi-impedance	

FIGURE 10-1: LOAD CONDITIONS - PIC16C52



10.4 Timing Diagrams and Specifications

FIGURE 10-2: EXTERNAL CLOCK TIMING - PIC16C52

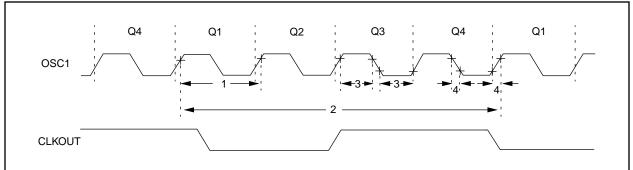


TABLE 10-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C52

AC Chara	cteristics	$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ (commercial)} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ (industrial)} \\ \mbox{Operating Voltage VDD range is described in Section 10.1.} \end{array}$							
Parameter No.	Sym	Sym Characteristic Min Typ ⁽¹⁾ Max Units			Conditions				
	Fosc	External CLKIN Frequency ⁽²⁾	DC	_	4	MHz	XT osc mode		
		Oscillator Frequency ⁽²⁾	DC	_	4	MHz	RC osc mode		
			0.1	_	4	MHz	XT osc mode		
1	Tosc	External CLKIN Period ⁽²⁾	250	_	—	ns	RC osc mode		
			250	_	—	ns	XT osc mode		
		Oscillator Period ⁽²⁾	250	_	—	ns	RC osc mode		
			250	_	10,000	ns	XT osc mode		
2	Тсү	Instruction Cycle Time ⁽³⁾	—	4/Fosc	—	_			
3	TosL, TosH	Clock in (OSC1) Low or High Time	85*	_	—	ns	XT oscillator		
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	_	_	25*	ns	XT oscillator		

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 10-3: CLKOUT AND I/O TIMING - PIC16C52

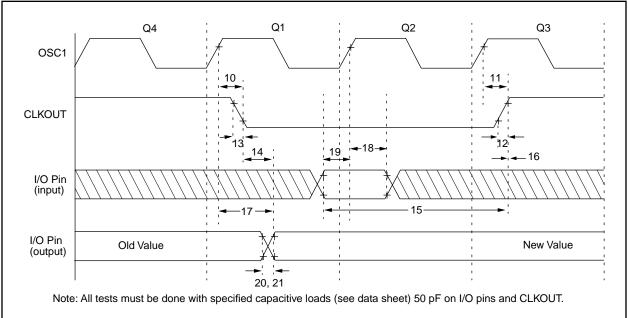


TABLE 10-2:CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C52

AC Chara	cteristics	Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ (commercial) $-40^{\circ}C \le TA \le +85^{\circ}C$ (industrial)Operating Voltage VDD range is described in Section 10.1.						
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units		
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽²⁾	—	15	30**	ns		
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽²⁾	_	15	30**	ns		
12	TckR	CLKOUT rise time ⁽²⁾	_	5	15**	ns		
13	TckF	CLKOUT fall time ⁽²⁾	_	5	15**	ns		
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽²⁾	_		40**	ns		
15	TioV2ckH	Port in valid before CLKOUT ⁽²⁾	0.25 TCY+30*		_	ns		
16	TckH2ioI	Port in hold after CLKOUT ⁽²⁾	0*		_	ns		
17	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port out valid ⁽³⁾	_		100*	ns		
18	TosH2iol	OSC1 [↑] (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	-	—	ns		
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	-	_	ns		
20	TioR	Port output rise time ⁽³⁾	_	10	25**	ns		
21	TioF	Port output fall time ⁽³⁾	—	10	25**	ns		

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

3: See Figure 10-1 for loading conditions.

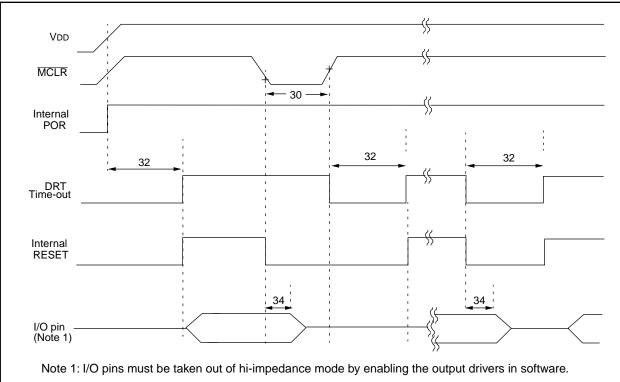


FIGURE 10-4: RESET AND DEVICE RESET TIMER TIMING - PIC16C52

TABLE 10-3: RESET AND DEVICE RESET TIMER - PIC16C52

AC Charact	racteristicsStandard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}C \leq TA \leq +70^{\circ}C$ (commercial) $-40^{\circ}C \leq TA \leq +85^{\circ}C$ (industrial) Operating Voltage VDD range is described in Section 10.1.						
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	100*		_	ns	VDD = 5 V
32	Tdrt	Device Reset Timer Period	9*	18*	30*	ms	VDD = 5 V (Commercial)
34	Tioz	I/O Hi-impedance from MCLR Low			100*	ns	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 10-5: TIMER0 CLOCK TIMINGS - PIC16C52

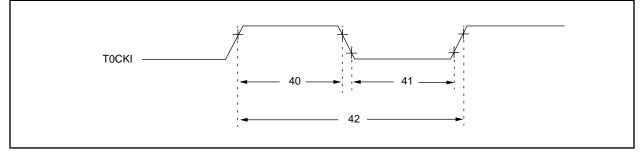


TABLE 10-4:TIMER0 CLOCK REQUIREMENTS - PIC16C52

AC	Charao	Operating Tempera	$\begin{array}{ll} \mbox{ng Conditions (unless otherwise specified)} \\ \mbox{iture} & 0^\circ C \leq T A \leq +70^\circ C \ (commercial) \\ & -40^\circ C \leq T A \leq +85^\circ C \ (industrial) \\ \mbox{VDD range is described in Section 10.1.} \end{array}$				
Parameter No.	Sym	Characteristic	Min	Тур ⁽¹⁾	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	_	_	ns	
		- With Prescaler	10*	_	_	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	_	_	ns	
		- With Prescaler	10*	_	_	ns	
42	Tt0P	T0CKI Period	20 or <u>Tcy + 40</u> * N	—	_	ns	Whichever is greater. N = Prescale Value (1, 2, 4,, 256)

^{*} These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

11.0 ELECTRICAL CHARACTERISTICS - PIC16C54/55/56/57

Absolute Maximum Ratings†

5	
Ambient Temperature under bias	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on VDD with respect to Vss	0V to +7.5V
Voltage on MCLR with respect to Vss ⁽²⁾	0V to +14V
Voltage on all other pins with respect to Vss	0.6V to (VDD + 0.6V)
Total Power Dissipation ⁽¹⁾	800 mW
Max. Current out of Vss pin	150 mA
Max. Current into VDD pin	100 mA
Max. Current into an input pin (T0CKI only)	
Input Clamp Current, Iк (VI < 0 or VI > VDD)	±20 mA
Output Clamp Current, IOK (VO < 0 or VO > VDD)	±20 mA
Max. Output Current sunk by any I/O pin	25 mA
Max. Output Current sourced by any I/O pin	20 mA
Max. Output Current sourced by a single I/O port (PORTA, B or C)	40 mA
Max. Output Current sunk by a single I/O port (PORTA, B or C)	50 mA
Note 1: Power Dissipation is calculated as follows: Pdis = VDD x {IDD $-\Sigma$ IOH} + Σ {(VDD	- VOH) x IOH} + Σ (VOL x IOL)
Note 2: Voltage spikes below Vss at the MCLR pin, inducing currents greater than 80 m	A, may cause latch-up. Thus.

Note 2: Voltage spikes below Vss at the $\overline{\text{MCLR}}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50 to 100 Ω should be used when applying a "low" level to the $\overline{\text{MCLR}}$ pin rather than pulling this pin directly to Vss

[†]NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 11-1:CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS
(RC, XT & 10) AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C5X-RC	PIC16C5X-XT	PIC16C5X-10
RC	VDD: 3.0 V to 6.25 V IDD: 3.3 mA max. at 5. V IPD: 9 μA max. at 3.0 V, WDT dis Freq: 4 MHz max.	N/A	N/A
хт	VDD: 3.0V to 6.25V IDD: 1.8 mA typ. at 5.5V IPD: 0.6 μA typ. at 3.0V WDT dis Freq: 4 MHz max.	VDD: 3.0V to 6.25V IDD: 3.3 mA max. at 5.5V IPD: 9 μA max. at 3.0V, WDT dis Freq: 4 MHz max.	N/A
HS	N/A	N/A	VDD: 4.5V to 5.5V IDD: 10 mA max. at 5.5V IPD: 9 μA max. at 3.0V, WDT dis Freq: 10 MHz max.
LP	VDD: 2.5V to 6.25V IDD: 15 μA typ. at 3.0V IPD: 0.6 μA typ. at 3.0V, WDT dis Freq: 40 kHz max.	VDD: 2.5V to 6.25V IDD: 15 μA typ. at 3.0V IPD: 0.6 μA typ. at 3.0V, WDT dis Freq: 40 kHz max.	VDD: 2.5V to 6.25V IDD: 15 μA typ. at 3.0V IPD: 0.6 μA typ. at 3.0V, WDT dis Freq: 40 kHz max.

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

TABLE 11-2:CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS
(HS, LP & JW) AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C5X-HS	PIC16C5X-LP	PIC16C5X/JW
RC	N/A	N/A	VDD: 3.0V to 6.25V IDD: 3.3 mA max. at 5.5V IPD: 9 μA max. at 3.0V, WDT dis Freq: 4 MHz max.
хт	N/A	N/A	VDD: 3.0V to 6.25V IDD: 3.3 mA max. at 5.5V IPD: 9 μA max. at 3.0V, WDT dis Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V IPD: 9 μA max. at 3.0V, WDT dis Freq: 20 MHz max.	N/A	VDD: 4.5V to 5.5V IDD: 20 mA max. at 5.5V IPD: 9 μA max. at 3.0V, WDT dis Freq: 20 MHz max.
LP	VDD: 2.5V to 6.25V IDD: 15 μA typ. at 3.0V IPD: 0.6 μA typ. at 3.0V, WDT dis Freq: 40 kHz max.	VDD: 2.5V to 6.25V IDD: 32 μA max. at 32 kHz, 3.0V IPD: 9 μA max. at 3.0V, WDT dis Freq: 40 kHz max.	VDD: 2.5V to 6.25V IDD: 32 μA max. at 32 kHz, 3.0V IPD: 9 μA max. at 3.0V, WDT dis Freq: 40 kHz max.

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

11.1 DC Characteristics: PIC16C5X-RC, XT, 10, HS, LP (Commercial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$							
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions			
Supply Voltage	Vdd								
PIC16C5X-RC		3.0		6.25	V	Fosc = DC to 4 MHz			
PIC16C5X-XT		3.0		6.25	V	Fosc = DC to 4 MHz			
PIC16C5X-10		4.5		5.5	V	Fosc = DC to 10 MHz			
PIC16C5X-HS		4.5		5.5	V	Fosc = DC to 20 MHz			
PIC16C5X-LP		2.5		6.25	V	Fosc = DC to 40 kHz			
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP Mode			
VDD Start Voltage to ensure Power-On Reset	VPOR		Vss		V	See Section 7.4 for details on Power-On Reset			
VDD Rise Rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-On Reset			
Supply Current ⁽³⁾	IDD								
PIC16C5X-RC ⁽⁴⁾			1.8	3.3	mA	Fosc = 4 MHz, VDD = 5.5V			
PIC16C5X-XT			1.8	3.3	mA	Fosc = 4 MHz, VDD = 5.5V			
PIC16C5X-10			4.8	10	mA	Fosc = 10 MHz, VDD = 5.5V			
PIC16C5X-HS			4.8	10	mA	Fosc = 10 MHz, VDD = 5.5V			
			9.0	20	mA	Fosc = 20 MHz, VDD = 5.5V			
PIC16C5X-LP			15	32	μA	Fosc = 32 kHz, VDD = 3.0V,			
						WDT disabled			
Power Down Current ⁽⁵⁾	IPD								
			4.0	12	μA	VDD = 3.0V, WDT enabled			
			0.6	9	μA	VDD = 3.0V, WDT disabled			

* These parameters are characterized but not tested.

- Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
 - 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to
 - V_{ss} , TOCKI = VDD, \overline{MCLR} = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
 - 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
 - 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

11.2 DC Characteristics: PIC16C5X-RCI, XTI, 10I, HSI, LPI (Industrial)

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}C \le TA \le +85^{\circ}C$							
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions		
Supply Voltage	Vdd							
PIC16C5X-RCI		3.0		6.25	V	Fosc = DC to 4 MHz		
PIC16C5X-XTI		3.0		6.25	V	Fosc = DC to 4 MHz		
PIC16C5X-10I		4.5		5.5	V	Fosc = DC to 10 MHz		
PIC16C5X-HSI		4.5		5.5	V	Fosc = DC to 20 MHz		
PIC16C5X-LPI		2.5		6.25	V	Fosc = DC to 40 kHz		
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP mode		
VDD Start Voltage to ensure Power-On Reset	VPOR		Vss		V	See Section 7.4 for details on Power-On Reset		
VDD Rise Rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-On Reset		
Supply Current ⁽³⁾	IDD							
PIC16C5X-RCI ⁽⁴⁾			1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V		
PIC16C5X-XTI			1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V		
PIC16C5X-10I			4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V		
PIC16C5X-HSI			4.8	10	mA	Fosc = 10 MHz, VDD = 5.5V		
			9.0	20	mA	Fosc = 20 MHz, VDD = 5.5V		
PIC16C5X-LPI			15	40	μA	FOSC = 32 kHz, VDD = 3.0 V,		
						WDT disabled		
Power Down Current ⁽⁵⁾	IPD							
			4.0	14	μA	VDD = 3.0V, WDT enabled		
			0.6	12	μA	VDD = 3.0V, WDT disabled		

* These parameters are characterized but not tested.

- Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
 - 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled toVss, TOCKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
 - 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
 - 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

11.3 DC Characteristics: PIC16C5X-RCE, XTE, 10E, HSE, LPE (Extended)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$						
Characteristic	Sym	Min	Тур ⁽¹⁾	Max	Units	Conditions		
Supply Voltage	Vdd							
PIC16C5X-RCE		3.25		6.0	V	Fosc = DC to 4 MHz		
PIC16C5X-XTE		3.25		6.0	V	Fosc = DC to 4 MHz		
PIC16C5X-10E		4.5		5.5	V	Fosc = DC to 10 MHz		
PIC16C5X-HSE		4.5		5.5	V	Fosc = DC to 16 MHz		
PIC16C5X-LPE		2.5		6.0	V	Fosc = DC to 40 kHz		
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP mode		
VDD Start Voltage to ensure Power-On Reset	VPOR		Vss		V	See Section 7.4 for details on Power-On Reset		
VDD rise rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-On Reset		
Supply Current ⁽³⁾	IDD							
PIC16C5X-RCE ⁽⁴⁾			1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V		
PIC16C5X-XTE			1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V		
PIC16C5X-10E			4.8	10	mA	Fosc = 10 MHz, VDD = 5.5V		
PIC16C5X-HSE			4.8	10	mA	Fosc = 10 MHz, VDD = 5.5V		
			9.0	20	mA	Fosc = 16 MHz, VDD = 5.5V		
PIC16C5X-LPE			19	55	μA	Fosc = 32 kHz, VDD = 3.25V,		
						WDT disabled		
Power Down Current ⁽⁵⁾	IPD							
			5.0	22	μA	VDD = 3.25V, WDT enabled		
			0.8	18	μA	VDD = 3.25V, WDT disabled		

* These parameters are characterized but not tested.

- Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
 - 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to
 - V_{ss} , TOCKI = VDD, \overline{MCLR} = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
 - 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
 - 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

11.4 DC Characteristics: PIC16C5X-RC, XT, 10, HS, LP (Commercial) PIC16C5X-RCI, XTI, 10I, HSI, LPI (Industrial)

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \leq TA \leq +70^{\circ}C$ (commercial) $-40^{\circ}C \leq TA \leq +85^{\circ}C$ (industrial)Operating Voltage VDD range is described in Section 11.1, Section 11.2 arSection 11.3.					
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions	
Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger)	VIL	Vss Vss Vss Vss Vss		0.2 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V V	Pin at hi-impedance PIC16C5X-RC only ⁽⁴⁾ PIC16C5X-XT, 10, HS, LP	
Input High Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger)	Viн	0.45 VDD 2.0 0.36 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD		VDD VDD VDD VDD VDD VDD VDD	V V V V V V	For all $V_{DD}^{(5)}$ 4.0V < $V_{DD} \le 5.5V^{(5)}$ $V_{DD} > 5.5V$ PIC16C5X-RC only ⁽⁴⁾ PIC16C5X-XT, 10, HS, LP	
Hysteresis of Schmitt Trigger inputs	VHYS	0.15Vdd*			V		
Input Leakage Current ^(2,3) I/O ports MCLR T0CKI OSC1	Ιι∟	-1 -5 -3 -3	0.5 0.5 0.5 0.5	+1 +5 +3 +3	μΑ μΑ μΑ μΑ	$\label{eq:ForVDD} \begin{split} & \textbf{For VDD} \leq \textbf{5.5V} \\ & \text{VSS} \leq \text{VPIN} \leq \text{VDD}, \\ & \text{Pin at hi-impedance} \\ & \text{VPIN} = \text{VSS} + 0.25\text{V} \\ & \text{VPIN} = \text{VDD} \\ & \text{VSS} \leq \text{VPIN} \leq \text{VDD} \\ & \text{VSS} \leq \text{VPIN} \leq \text{VDD} \\ & \text{VSS} \leq \text{VPIN} \leq \text{VDD}, \\ & \text{PIC16C5X-XT, 10, HS, LP} \end{split}$	
Output Low Voltage I/O ports OSC2/CLKOUT	Vol			0.6 0.6	V V	IOL = 8.7 mA, VDD = 4.5V IOL = 1.6 mA, VDD = 4.5V, PIC16C5X-RC	
Output High Voltage I/O ports ⁽³⁾ OSC2/CLKOUT	Vон	Vdd - 0.7 Vdd - 0.7			V V	IOH = -5.4 mA, VDD = 4.5V IOH = -1.0 mA, VDD = 4.5V, PIC16C5X-RC	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

11.5 DC Characteristics: PIC16C5X-RC, XT, 10, HS, LP (Extended)

DC Characteristics All Pins Except Power Supply Pins		Operating Te	emperature	e –40°C≤	TA ≤ +12	herwise specified) 25°C Section 11.1, Section 11.2 and
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions
Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger)	VIL	Vss Vss Vss Vss Vss		0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V V	Pin at hi-impedance PIC16C5X-RC only ⁽⁴⁾ PIC16C5X-XT, 10, HS, LP
Input High Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger)	Viн	0.45 VDD 2.0 0.36 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD		VDD VDD VDD VDD VDD VDD VDD	V V V V V V	For all VDD ⁽⁵⁾ $4.0V < VDD \le 5.5V^{(5)}$ VDD > 5.5 V PIC16C5X-RC only ⁽⁴⁾ PIC16C5X-XT, 10, HS, LP
Hysteresis of Schmitt Trigger inputs	VHYS	0.15Vdd*			V	
Input Leakage Current ^(2,3) I/O ports MCLR T0CKI OSC1	IIL.	-1 -5 -3 -3	0.5 0.5 0.5 0.5	+1 +5 +3 +3	μΑ μΑ μΑ μΑ μΑ	$\label{eq:starsest} \begin{array}{l} \mbox{For VDD} \leq 5.5 \ V \\ \mbox{Vss} \leq \mbox{VPIN} \leq \mbox{VDD}, \\ \mbox{Pin at hi-impedance} \\ \mbox{VPIN} = \ V\mbox{Vss} + 0.25 \ V \\ \mbox{VPIN} = \ V\mbox{DD} \\ \mbox{Vss} \leq \ V\mbox{PIN} \leq \ V\mbox{DD} \\ \mbox{Vss} \leq \ V\mbox{PIN} \leq \ V\mbox{DD}, \\ \mbox{PIC16C5X-XT}, \ 10, \ H\mbox{S}, \ L\mbox{P} \end{array}$
Output Low Voltage I/O ports OSC2/CLKOUT	Vol			0.6 0.6	V V	IOL = 8.7 mA, VDD = 4.5V IOL = 1.6 mA, VDD = 4.5V, PIC16C5X-RC
Output High Voltage I/O ports ⁽³⁾ OSC2/CLKOUT	Vон	Vdd - 0.7 Vdd - 0.7			V V	IOH = -5.4 mA, VDD = 4.5V IOH = -1.0 mA, VDD = 4.5V, PIC16C5X-RC

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

- 4: For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.
- 5: The user may use the better of the two specifications.

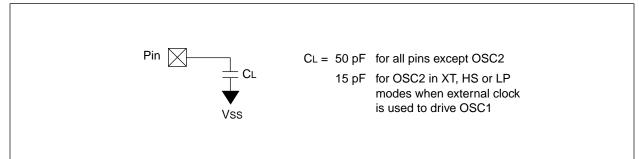
11.6 <u>Timing Parameter Symbology and Load Conditions</u>

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS

2. TppS				
Т				
F	Frequency	Т	Time	
Lowerc	ase subscripts (pp) and their meanings	:		
рр				
2	to	mc	MCLR	
ck	CLKOUT	OSC	oscillator	
су	cycle time	OS	OSC1	
drt	device reset timer	tO	TOCKI	
io	I/O port	wdt	watchdog timer	
Upperc	case letters and their meanings:			
S				
F	Fall	P	Period	
н	High	R	Rise	
1	Invalid (Hi-impedance)	V	Valid	
L	Low	Z	Hi-impedance	

FIGURE 11-1: LOAD CONDITIONS - PIC16C54/55/56/57



11.7 Timing Diagrams and Specifications

FIGURE 11-2: EXTERNAL CLOCK TIMING - PIC16C54/55/56/57

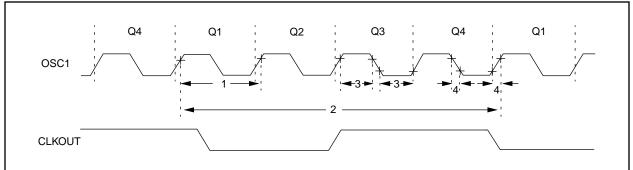


TABLE 11-3: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54/55/56/57

AC CharacteristicsStandard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ (commercial) $-40^{\circ}C \le TA \le +85^{\circ}C$ (industrial) $-40^{\circ}C \le TA \le +125^{\circ}C$ (extended) Operating Voltage VDD range is described in Section 11.1, Section 11.2 and S							
Parameter No.	Sym	Characteristic	Characteristic Min Typ ⁽¹⁾ Max Units Condit				
	Fosc	External CLKIN Frequency ⁽²⁾	DC	_	4	MHz	XT osc mode
			DC	_	10	MHz	10 MHz mode
			DC	_	20	MHz	HS osc mode (Com/Indust)
			DC	_	16	MHz	HS osc mode (Extended)
			DC	_	40	kHz	LP osc mode
		Oscillator Frequency ⁽²⁾	DC	_	4	MHz	RC osc mode
			0.1	_	4	MHz	XT osc mode
			4	_	10	MHz	10 MHz mode
			4	_	20	MHz	HS osc mode (Com/Indust)
			4	_	16	MHz	HS osc mode (Extended)
			DC	_	40	kHz	LP osc mode
* These pa	Irameters are	Oscillator Frequency ⁽²⁾	0.1 4 4 4		4 10 20 16	MHz MHz MHz MHz	XT osc mode 10 MHz mode HS osc mode (Com/Indust) HS osc mode (Extended)

These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

TABLE 11-3: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54/55/56/57 (CON'T)

AC CharacteristicsStandard Operating Conditions (unless otherwise s Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ (comme $-40^{\circ}C \le TA \le +85^{\circ}C$ (industriant $-40^{\circ}C \le TA \le +125^{\circ}C$ (extern Operating Voltage VDD range is described in Section 11					ercial) rial) nded)		
Parameter No.	Sym	Characteristic	Min	Тур ⁽¹⁾	Max	Units	Conditions
1	Tosc	External CLKIN Period ⁽²⁾	250	_	—	ns	XT osc mode
			100	_	_	ns	10 MHz mode
			50	_	_	ns	HS osc mode (Com/Indust)
			62.5	—	_	ns	HS osc mode (Extended)
			25	—	_	μs	LP osc mode
		Oscillator Period ⁽²⁾	250	_	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			100	—	250	ns	10 MHz mode
			50	—	250	ns	HS osc mode (Com/Indust)
			62.5	—	250	ns	HS osc mode (Extended)
			25	—	—	μs	LP osc mode
2	Тсү	Instruction Cycle Time ⁽³⁾	—	4/Fosc	—	_	
3	TosL, TosH	Clock in (OSC1) Low or High Time	85*	_		ns	XT oscillator
			20*	_	_	ns	HS oscillator
			2*	_	_	μs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	_	_	25*	ns	XT oscillator
			_	_	25*	ns	HS oscillator
			_	_	50*	ns	LP oscillator

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 11-3: CLKOUT AND I/O TIMING - PIC16C54/55/56/57

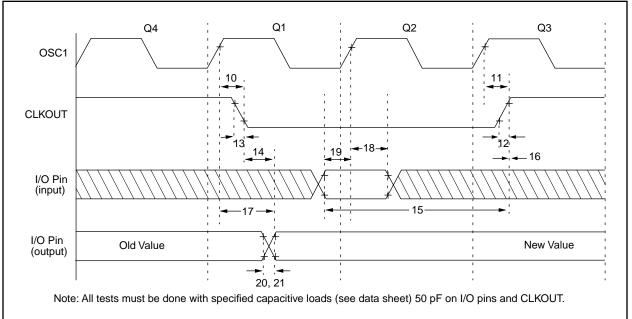


TABLE 11-4:	CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54/55/56/57
-------------	--

AC Chara	cteristics	$\begin{array}{llllllllllllllllllllllllllllllllllll$					
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽²⁾		15	30**	ns	
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽²⁾	_	15	30**	ns	
12	TckR	CLKOUT rise time ⁽²⁾	_	5	15**	ns	
13	TckF	CLKOUT fall time ⁽²⁾	_	5	15**	ns	
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽²⁾	—	_	40**	ns	
15	TioV2ckH	Port in valid before CLKOUT ⁽²⁾	0.25 TCY+30*	_	_	ns	
16	TckH2iol	Port in hold after CLKOUT ⁽²⁾	0*	_	_	ns	
17	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port out valid ⁽³⁾	_	_	100*	ns	
18	TosH2iol	OSC1 [↑] (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	-	_	ns	
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	-	_	ns	
20	TioR	Port output rise time ⁽³⁾	_	10	25**	ns	
21	TioF	Port output fall time ⁽³⁾	_	10	25**	ns	

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

3: See Figure 11-1 for loading conditions.

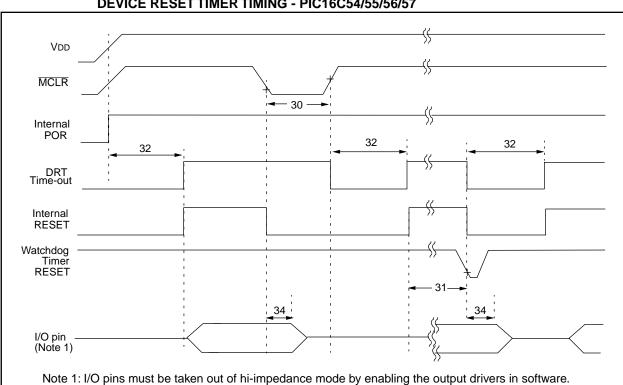


FIGURE 11-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54/55/56/57

TABLE 11-5: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54/55/56/57

AC CharacteristicsStandard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ (commercial) $-40^{\circ}C \le TA \le +85^{\circ}C$ (industrial) $-40^{\circ}C \le TA \le +125^{\circ}C$ (extended) Operating Voltage VDD range is described in Section 11.1, Section 11.2 and					11.2 and Section 11.3		
Parameter No.	Sym	Characteristic Min Typ ⁽¹⁾ Max Units				Conditions	
30	TmcL	MCLR Pulse Width (low)	100*	_		ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9*	18*	30*	ms	VDD = 5.0V (Commercial)
32	Tdrt	Device Reset Timer Period	9*	18*	30*	ms	VDD = 5.0V (Commercial)
34	Tioz	I/O Hi-impedance from MCLR Low	_	_	100*	ns	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 11-5: TIMER0 CLOCK TIMINGS - PIC16C54/55/56/57

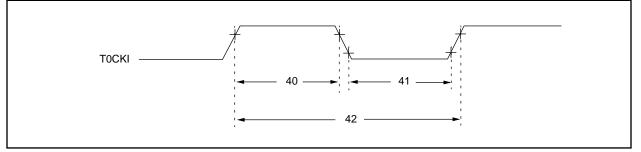


TABLE 11-6: TIMER0 CLOCK REQUIREMENTS - PIC16C54/55/56/57

AC	Charao	haracteristicsStandard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}C \leq TA \leq +70^{\circ}C$ (commercial) $-40^{\circ}C \leq TA \leq +85^{\circ}C$ (industrial) $-40^{\circ}C \leq TA \leq +125^{\circ}C$ (extended) Operating Voltage VDD range is described in Section 11.1, Section 11 Section 11.3						ercial) ial) ded)
Parameter No.	Sym	Characteristic		Min	Typ ⁽¹⁾	Мах	Units	Conditions
40	Tt0H	T0CKI High Pulse \	Width - No Prescaler	0.5 TCY + 20*	—	_	ns	
			- With Prescaler	10*	_	_	ns	
41	Tt0L	T0CKI Low Pulse V	Vidth - No Prescaler	0.5 TCY + 20*	_	_	ns	
			- With Prescaler	10*	_	_	ns	
42	Tt0P	T0CKI Period		20 or <u>Tcy + 40</u> * N		_	ns	Whichever is greater. N = Prescale Value (1, 2, 4,, 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

NOTES:

12.0 DC AND AC CHARACTERISTICS - PIC16C54/55/56/57

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean - 3σ) respectively, where σ is standard deviation.

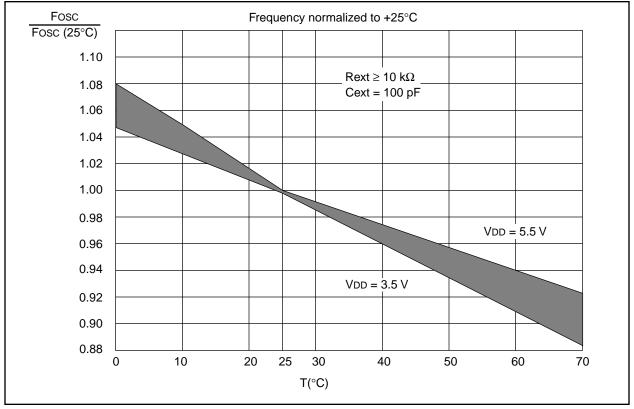


FIGURE 12-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

TABLE 12-1:	RC OSCILLATOR FREQUENCIES
-------------	----------------------------------

Cext	Rext	Average Fosc @ 5V, 25°C			
20 pF	3.3 k	4.973 MHz	± 27%		
	5 k	3.82 MHz	± 21%		
	10 k	2.22 MHz	± 21%		
	100 k	262.15 kHz	± 31%		
100 pF	3.3 k	1.63 MHz	± 13%		
	5 k	1.19 MHz	± 13%		
	10 k	684.64 kHz	± 18%		
	100 k	71.56 kHz	± 25%		
300 pF	3.3 k	660 kHz	± 10%		
	5.0 k	484.1 kHz	± 14%		
	10 k	267.63 kHz	± 15%		
	160 k	29.44 kHz	± 19%		

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ± 3 standard deviation from average value for VDD = 5 V.

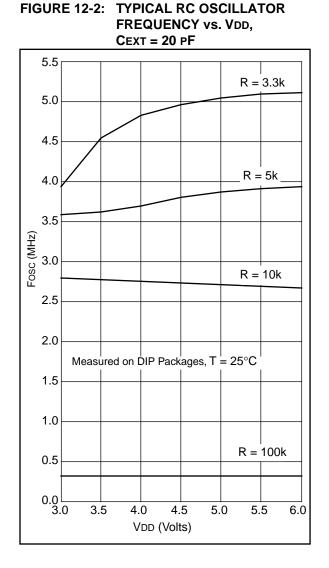


FIGURE 12-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 100 PF

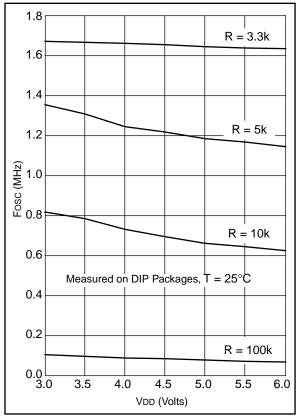


FIGURE 12-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 PF

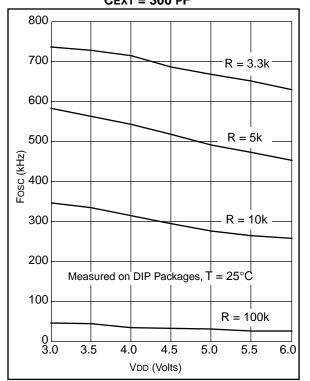


FIGURE 12-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED

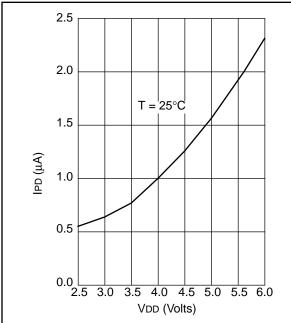


FIGURE 12-6: MAXIMUM IPD vs. VDD, WATCHDOG DISABLED

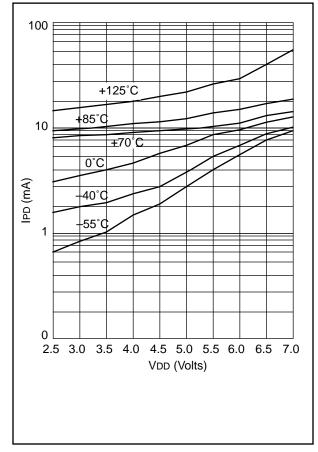


FIGURE 12-7: TYPICAL IPD vs. VDD, WATCHDOG ENABLED

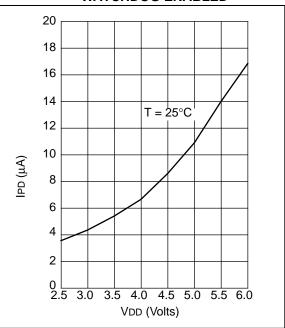
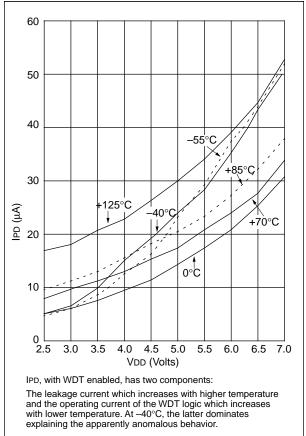


FIGURE 12-8: MAXIMUM IPD vs. VDD, WATCHDOG ENABLED



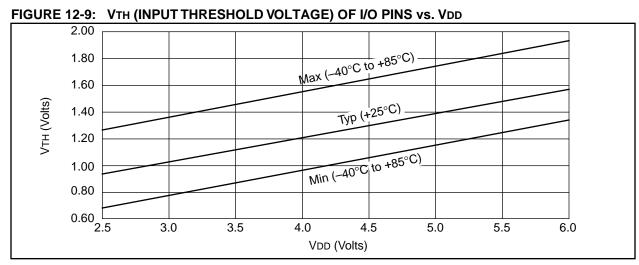


FIGURE 12-10: VIH, VIL OF MCLR, TOCKI AND OSC1 (IN RC MODE) vs. VDD

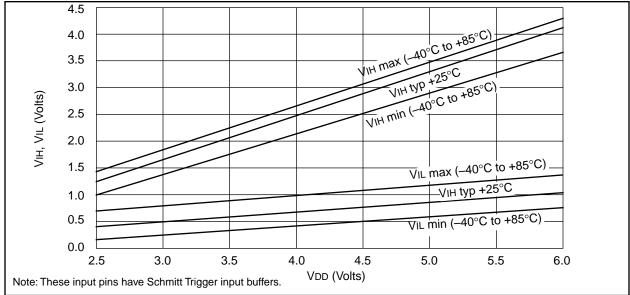
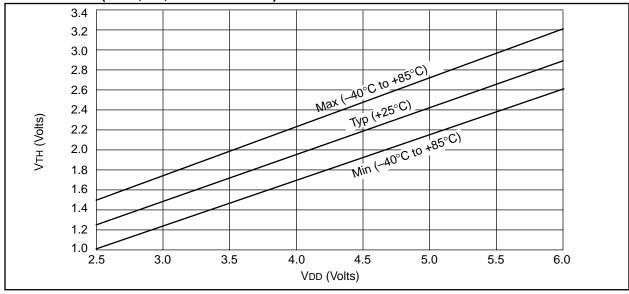
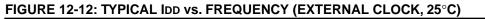
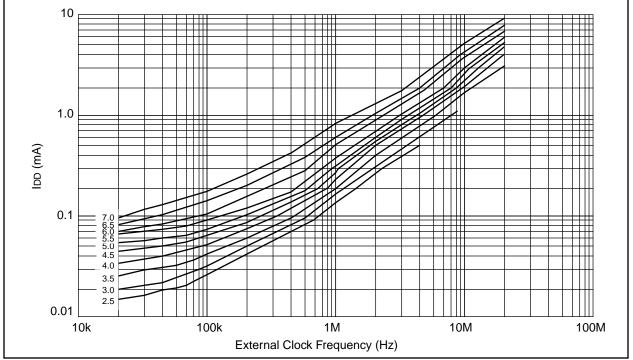


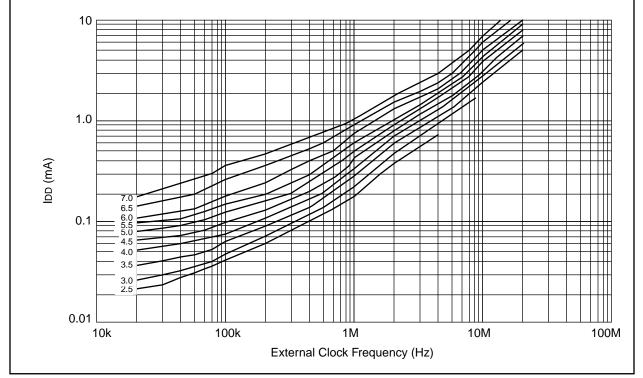
FIGURE 12-11: VTH (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs. VDD













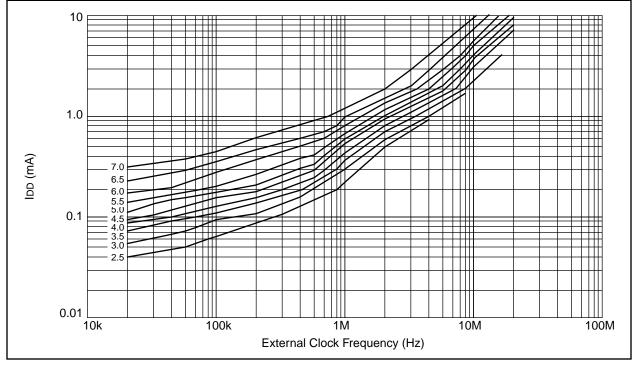
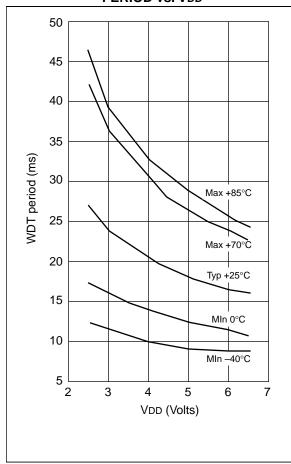
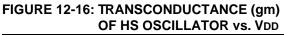
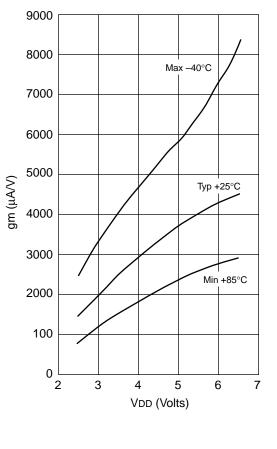


FIGURE 12-15: WDT TIMER TIME-OUT PERIOD vs. VDD







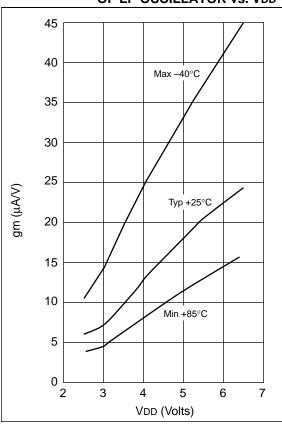
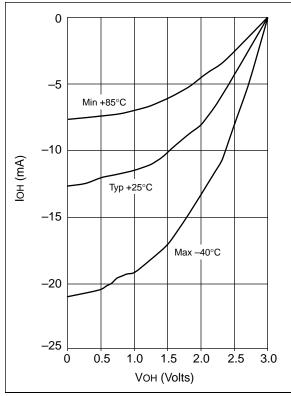
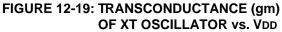


FIGURE 12-17: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD

FIGURE 12-18: IOH vs. VOH, VDD = 3 V





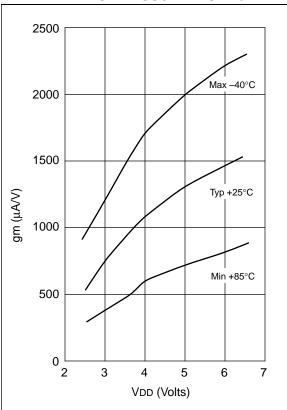


FIGURE 12-20: IOH vs. VOH, VDD = 5 V

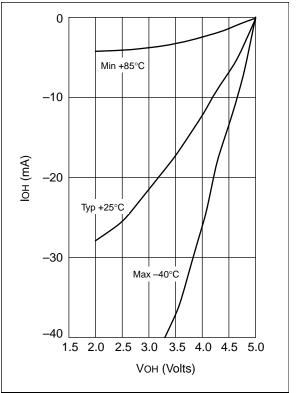


FIGURE 12-21: IOL vs. VOL, VDD = 3 V

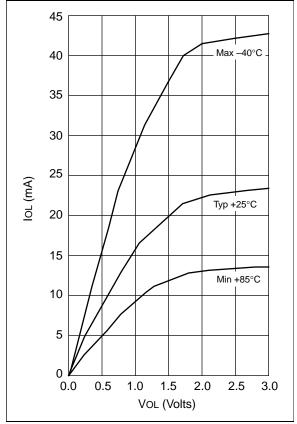


TABLE 12-2:INPUT CAPACITANCE FOR
PIC16C54/56

Pin	Typical Capacitance (pF)				
FIII	18L PDIP	18L SOIC			
RA port	5.0	4.3			
RB port	5.0	4.3			
MCLR	17.0	17.0			
OSC1	4.0	3.5			
OSC2/CLKOUT	4.3	3.5			
ТОСКІ	3.2	2.8			

All capacitance values are typical at 25°C. A part-to-part variation of \pm 25% (three standard deviations) should be taken into account.

FIGURE 12-22: IOL vs. VOL, VDD = 5 V

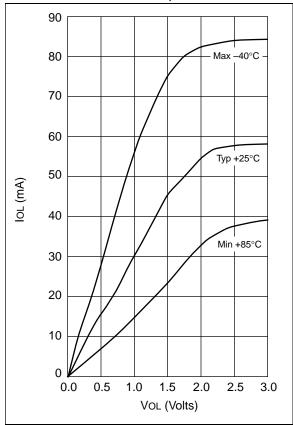


TABLE 12-3:INPUT CAPACITANCE FOR
PIC16C55/57

	Typical Capacitance (pF)					
Pin	28L PDIP (600 mil)	28L SOIC				
RA port	5.2	4.8				
RB port	5.6	4.7				
RC port	5.0	4.1				
MCLR	17.0	17.0				
OSC1	6.6	3.5				
OSC2/CLKOUT	4.6	3.5				
ТОСКІ	4.5	3.5				

All capacitance values are typical at 25°C. A part-to-part variation of $\pm 25\%$ (three standard deviations) should be taken into account.

13.0 ELECTRICAL CHARACTERISTICS - PIC16CR54A

Absolute Maximum Ratings†

Ambient Temperature under bias	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on VDD with respect to Vss	0 to +7.5V
Voltage on MCLR with respect to Vss ⁽²⁾	0 to +14V
Voltage on all other pins with respect to Vss	–0.6V to (VDD + 0.6V)
Total Power Dissipation ⁽¹⁾	800 mW
Max. Current out of Vss pin	
Max. Current into VDD pin	
Max. Current into an input pin (T0CKI only)	±500 μA
Input Clamp Current, Iк (VI < 0 or VI > VDD)	±20 mA
Output Clamp Current, IOK (V0 < 0 or V0 > VDD)	
Max. Output Current sunk by any I/O pin	25 mA
Max. Output Current sourced by any I/O pin	20 mA
Max. Output Current sourced by a single I/O port (PORTA or B)	40 mA
Max. Output Current sunk by a single I/O port (PORTA or B)	50 mA
Note 1: Power Dissipation is calculated as follows: PDIS = VDD x {IDD - \sum IOH} + \sum {(VDD-	Voh) x Ioh} + Σ (Vol x Iol)
Note 2: Voltage spikes below Ves at the \overline{MCLP} pip inducing surroute greater than 80 mA	mov oquaa latah up. Thua

Note 2: Voltage spikes below Vss at the $\overline{\text{MCLR}}$ pin, inducing currents greater than 80 mA may cause latch-up. Thus, a series resistor of 50 to 100 Ω should be used when applying a low level to the $\overline{\text{MCLR}}$ pin rather than pulling this pin directly to Vss.

[†]NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 13-1:CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS
AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16CR54A-04	PIC16CR54A-10	PIC16CR54A-20	PIC16LCR54A-04
RC	VDD: 2.5 V to 6.25 V IDD: 3.6 mA max at 6.0 V IPD: 6.0 μA max at 2.5 V, WDT dis Freq: 4 MHz max	N/A	N/A	N/A
ХТ	VDD: 2.5 V to 6.25 V IDD: 3.6 mA max at 6.0 V IPD: 6.0 μA max at 2.5 V, WDT dis Freq: 4.0 MHz max	N/A	N/A	N/A
HS	N/A	VDD: 4.5 V to 5.5 V IDD: 10 mA max at 5.5 V IPD: 6.0 μA max at 2.5 V, WDT dis Freq: 10 MHz max	VDD: 4.5 V to 5.5 V IDD: 10 mA max at 5.5 V IPD: 6.0 μA max at 2.5 V, WDT dis Freq: 20 MHz max	N/A
LP	N/A	N/A	N/A	VDD: 2.0 V to 6.25 V IDD: 20 μA max at 32 kHz, 2.0 V IPD: 6.0 μA max at 2.5 V, WDT dis Freq: 200 kHz max

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

13.1 DC Characteristics: PIC16CR54A-04, 10, 20 (Commercial) PIC16CR54A-04I, 10I, 20I (Industrial)

DC Characteristics Power Supply Pins	$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ (commercial)} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ (industrial)} \end{array}$						
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions	
Supply Voltage RC and XT options	Vdd	2.5		6.25	v		
HS option		4.5		5.5	V		
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP mode	
VDD Start Voltage to ensure Power-on Reset	VPOR		Vss		V	See Section 7.4 for details on Power-on Reset	
VDD Rise Rate to ensure Power-on Reset	Svdd	0.05*			V/ms	See Section 7.4 for details on Power-on Reset	
Supply Current ⁽³⁾	IDD						
RC ⁽⁴⁾ and XT options			2.0	3.6	mA	FOSC = 4.0 MHz, VDD = 6.0 V	
			0.8 90	1.8 350	mA	Fosc = 4.0 MHz, VDD = 3.0V	
HS option			90 4.8	10	μA mA	Fosc = 200 kHz, VDD = 2.5V Fosc = 10 MHz, VDD = 5.5V	
			9.0	20	mA	Fosc = 20 MHz, VDD = 5.5 V	
Power-Down Current ⁽⁵⁾ Commercial	IPD						
			1.0	6.0	μΑ	VDD = 2.5V, WDT disabled	
			2.0	8.0*	μΑ	VDD = 4.0V, WDT disabled	
			3.0 5.0	15 25	μΑ μΑ	VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled	
Power-Down Current ⁽⁵⁾ Industrial	IPD		0.0		μι		
			1.0	8.0	μA	VDD = 2.5V, WDT disabled	
			2.0	10*	μA	VDD = 4.0V, WDT disabled	
			3.0	20*	μA	VDD = 4.0V, WDT enabled	
			3.0	18	μA	VDD = 6.0V, WDT disabled	
			5.0	45	μA	VDD = 6.0V, WDT enabled	

* These parameters are characterized but not tested.

- Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
 - 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
 - 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
 - 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

13.2 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ (extended)						
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions	
Supply Voltage	Vdd						
RC and XT options		3.25		6.0	V		
HS options		4.5		5.5	V		
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP mode	
VDD Start Voltage to ensure Power-on Reset	VPOR		Vss		V	See Section 7.4 for details on Power-on Reset	
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset	
Supply Current ⁽³⁾	IDD						
RC ⁽⁴⁾ and XT options			1.8	3.3	mA	Fosc = 4.0 MHz, VDD = 5.5V	
HS option			4.8	10	mA	Fosc = 10 MHz, VDD = 5.5V	
			9.0	20	mA	Fosc = 16 MHz, VDD = 5.5V	
Power-Down Current ⁽⁵⁾	IPD						
			5.0	22	μA	VDD = 3.25V, WDT enabled	
			0.8	18	μA	VDD = 3.25V, WDT disabled	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
- 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
- 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
- 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

13.3 <u>DC Characteristics:</u> <u>PIC16LCR54A-04 (Commercial)</u> <u>PIC16LCR54A-04I (Industrial)</u>

DC Characteristics Power Supply Pins	$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ (commercial)} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ (industrial)} \end{array}$					
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions
Supply Voltage	Vdd	2.0		6.25	V	
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR		Vss		V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset
Supply Current ⁽³⁾	Idd		10	20 70	μΑ μΑ	Fosc = 32 kHz, VDD = 2.0V Fosc = 32 kHz, VDD = 6.0V
Power-Down Current ⁽⁵⁾ Commercial	IPD		1.0 2.0 3.0	6.0 8.0* 15	μΑ μΑ μΑ	VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 6.0V, WDT disabled
Power-Down Current ⁽⁵⁾ Industrial	IPD		5.0 1.0 2.0 3.0 3.0 5.0	25 8.0 10* 20* 18 45	μΑ μΑ μΑ μΑ μΑ μΑ	VDD = 6.0V, WDT enabled VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 4.0V, WDT enabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled

* These parameters are characterized but not tested.

- Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
 - 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are:
 - OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
 - 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
 - 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

13.4 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ (commercial) $-40^{\circ}C \le TA \le +85^{\circ}C$ (industrial)							
		Operating Voltage VDD range is described in Section 13.1 and Section 13.							
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions			
Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	VIL	Vss Vss Vss Vss Vss		0.2 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD	V V V V	Pin at hi-impedance RC option only ⁽⁴⁾ XT, HS and LP options			
Input High Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1 Hysteresis of Schmitt Trigger inputs	VIH	2.0 0.6 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.15VDD*		VDD VDD VDD VDD VDD VDD	V V V V V V	VDD = 3.0V to 5.5V ⁽⁵⁾ Full VDD range ⁽⁵⁾ RC option only ⁽⁴⁾ XT, HS and LP options			
Input Leakage Current ⁽³⁾ I/O ports MCLR T0CKI OSC1	lı∟	-1.0 -5.0 -3.0 -3.0	0.5 0.5 0.5	+1.0 +5.0 +3.0 +3.0	μΑ μΑ μΑ μΑ μΑ	$\label{eq:statestar} \begin{array}{l} \mbox{For VDD} \leq \mbox{5.5V} \\ \mbox{Vss} \leq \mbox{VpIN} \leq \mbox{VdD}, \\ \mbox{Pin at hi-impedance} \\ \mbox{VpIN} = \mbox{Vss} + 0.25 \mbox{V}^{(2)} \\ \mbox{VpIN} = \mbox{VdD}^{(2)} \\ \mbox{Vss} \leq \mbox{VpIN} \leq \mbox{VdD} \\ \mbox{Vss} \leq \mbox{VpIN} \leq \mbox{VdD}, \\ \mbox{XT, HS and LP options} \end{array}$			
Output Low Voltage I/O ports OSC2/CLKOUT Output High Voltage ⁽³⁾ I/O ports OSC2/CLKOUT	Vol	Vdd -0.5 Vdd -0.5		0.5 0.5	V V V	IOL = 10 mA, VDD = $6.0V$ IOL = 1.9 mA, VDD = $6.0V$, RC option only IOH = -4.0 mA, VDD = $6.0V$ IOH = -0.8 mA, VDD = $6.0V$, RC option only			

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

13.5 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

DC Characteristics All Pins Except Power Supply Pins		Operating Te	emperatu	ire -	-40°C ≤ 1	otherwise specified) Γa ≤ +125°C n Section 13.2.
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions
Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	VIL	Vss Vss Vss Vss Vss		0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V	Pin at hi-impedance RC option only ⁽⁴⁾ XT, HS and LP options
Input High Voltage I/O ports MCLR (Schmitt Trigger) TOCKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	Vih	0.45 VDD 2.0 0.36 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD		VDD VDD VDD VDD VDD VDD VDD VDD	V V V V V V	For all VDD ⁽⁵⁾ 4.0V < VDD \leq 5.5V ⁽⁵⁾ VDD > 5.5V RC option only ⁽⁴⁾ XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	VHYS	0.15Vdd*			V	
Input Leakage Current ⁽³⁾ I/O ports MCLR T0CKI OSC1	IIL.	-1.0 -5.0 -3.0 -3.0	0.5 0.5 0.5 0.5	+1.0 +5.0 +3.0 +3.0	μΑ μΑ μΑ μΑ	$\label{eq:statestar} \begin{array}{l} \mbox{For VDD} \leq 5.5V \\ \mbox{Vss} \leq \mbox{VpIN} \leq \mbox{VdD}, \\ \mbox{Pin at hi-impedance} \\ \mbox{VpIN} = \mbox{Vss} + 0.25 \mbox{V}^{(2)} \\ \mbox{VpIN} = \mbox{VdD}^{(2)} \\ \mbox{Vss} \leq \mbox{VpIN} \leq \mbox{VdD} \\ \mbox{Vss} \leq \mbox{VpIN} \leq \mbox{VdD}, \\ \mbox{XT, HS and LP options} \end{array}$
Output Low Voltage I/O ports OSC2/CLKOUT	Vol			0.6 0.6	V V	IOL = 8.7 mA, VDD = $4.5V$ IOL = 1.6 mA, VDD = $4.5V$, RC option only
Output High Voltage ⁽³⁾ I/O ports OSC2/CLKOUT	Vон	Vdd0.7 Vdd0.7			V V	IOH = -5.4 mA, $VDD = 4.5VIOH = -1.0$ mA, $VDD = 4.5V$, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

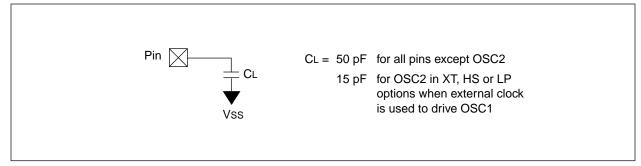
13.6 <u>Timing Parameter Symbology and Load Conditions</u>

The timing parameter symbols have been created following one of the following formats:

- 1. TppS2ppS
- 2. TppS

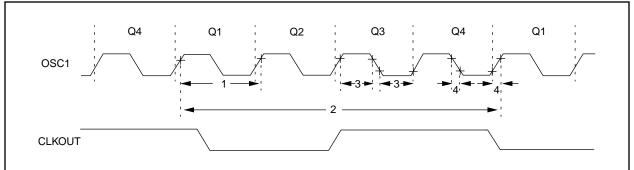
2. Tpp3			
т			
F	Frequency	Т	Time
Lowerc	ase subscripts (pp) and their meanings:		
рр			
2	to	mc	MCLR
ck	CLKOUT	osc	oscillator
су	cycle time	os	OSC1
drt	device reset timer	tO	TOCKI
io	I/O port	wdt	watchdog timer
Upperc	case letters and their meanings:		
S			
F	Fall	P	Period
н	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 13-1: LOAD CONDITIONS



13.7 **Timing Diagrams and Specifications**

FIGURE 13-2: EXTERNAL CLOCK TIMING - PIC16CR54A



EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR54A TABLE 13-2:

AC Characteristics		$ \begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ (commercial)} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ (industrial)} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ (extended)} \\ \mbox{Operating Voltage VDD range is described in Section 13.1, Section 13.2 and Section 13.3.} \end{array} $							
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions		
	Fosc	External CLKIN Frequency ⁽²⁾	DC	_	4.0	MHz	XT osc mode		
			DC	—	4.0	MHz	HS osc mode (04)		
			DC	—	10	MHz	HS osc mode (10)		
			DC	—	20	MHz	HS osc mode (20)		
			DC	—	200	kHz	LP osc mode		
		Oscillator Frequency ⁽²⁾	DC	Ι	4.0	MHz	RC osc mode		
			0.1	—	4.0	MHz	XT osc mode		
			4.0	—	4.0	MHz	HS osc mode (04)		
			4.0	—	10	MHz	HS osc mode (10)		
			4.0	—	20	MHz	HS osc mode (20)		
			5.0	—	200	kHz	LP osc mode		

These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

TABLE 13-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR54A (CON'T)

AC Chara	cteristics	$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ (commercial)} \\ & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ (industrial)} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ (extended)} \\ \mbox{Operating Voltage VDD range is described in Section 13.1, Section 13.2 and Section 13.3.} \end{array}$						
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions	
1	Tosc	External CLKIN Period ⁽²⁾	250	_	_	ns	XT osc mode	
			250	_	_	ns	HS osc mode (04)	
			100	_	_	ns	HS osc mode (10)	
			50	_	_	ns	HS osc mode (20)	
			5.0	_	—	μs	LP osc mode	
		Oscillator Period ⁽²⁾	250	_	—	ns	RC osc mode	
			250	_	10,000	ns	XT osc mode	
			250	-	250	ns	HS osc mode (04)	
			100	-	250	ns	HS osc mode (10)	
			50	—	250	ns	HS osc mode (20)	
			5.0	_	200	μs	LP osc mode	
2	Тсү	Instruction Cycle Time ⁽³⁾	—	4/Fosc	—			
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	_	—	ns	XT oscillator	
			20*	_		ns	HS oscillator	
			2.0*	_	_	μs	LP oscillator	
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	_	25*	ns	XT oscillator	
			_	_	25*	ns	HS oscillator	
			_	_	50*	ns	LP oscillator	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 13-3: CLKOUT AND I/O TIMING - PIC16CR54A

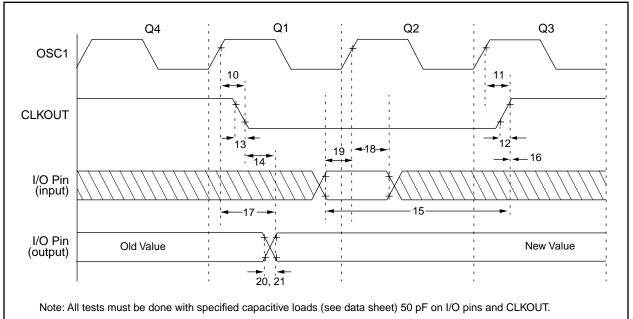


TABLE 13-3:	CLKOUT AND I/O TIMING REQUIREMENTS - PIC16CR54A

AC Chara	cteristics	$\begin{array}{llllllllllllllllllllllllllllllllllll$									
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units					
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽²⁾	_	15	30**	ns					
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽²⁾	_	15	30**	ns					
12	TckR	CLKOUT rise time ⁽²⁾	_	5.0	15**	ns					
13	TckF	CLKOUT fall time ⁽²⁾	_	5.0	15**	ns					
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽²⁾	—	_	40**	ns					
15	TioV2ckH	Port in valid before CLKOUT ⁽²⁾	0.25 TCY+30*	_	_	ns					
16	TckH2iol	Port in hold after CLKOUT ⁽²⁾	0*	_	_	ns					
17	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port out valid ⁽³⁾	_	_	100*	ns					
18	TosH2iol	OSC1 [↑] (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	-	_	ns					
19	TioV2osH	Port input valid to OSC1 [↑] (I/O in setup time)	TBD	-		ns					
20	TioR	Port output rise time ⁽³⁾	_	10	25**	ns					
21	TioF	Port output fall time ⁽³⁾	_	10	25**	ns					

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

3: See Figure 13-1 for loading conditions.

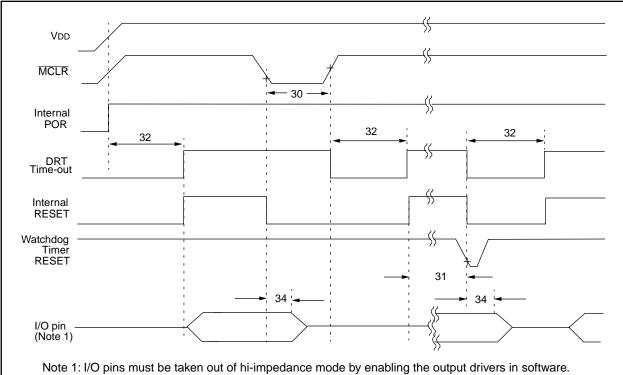


FIGURE 13-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16CR54A

TABLE 13-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16CR54A

AC Charac	teristics	$ \begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ (commercial)} \\ & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ (industrial)} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ (extended)} \\ \mbox{Operating Voltage VDD range is described in Section 13.1, Section 13.2 and Section 13.3.} \end{array} $							
Parameter No.	Sym	Characteristic Min Typ ⁽¹⁾ Max Units Conditions							
30	TmcL	MCLR Pulse Width (low)	1.0*	_		μs	VDD = 5.0V		
31	Twdt	Watchdog Timer Time-out Period 7.0^* 18^* 40^* ms $VDD = 5.0V$ (Commercial (No Prescaler)							
32	Tdrt	Device Reset Timer Period 7.0^* 18^* 30^* msVDD = $5.0V$ (Commercial)							
34	Tioz	I/O Hi-impedance from MCLR Low	_	_	1.0*	μs			

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 13-5: TIMER0 CLOCK TIMINGS - PIC16CR54A

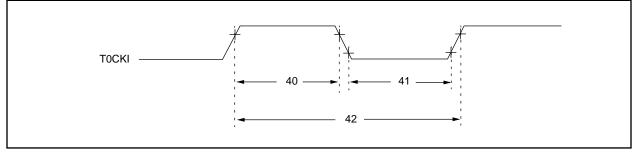


TABLE 13-5: TIMER0 CLOCK REQUIREMENTS - PIC16CR54A

AC	–40°C ≤ –40°C ≤	≦ TA ≤ + ≦ TA ≤ + ≦ TA ≤ +	70°C ∙85°C •125°C	(comme (industr C (exten	rial)			
Parameter No.	Sym	Characteristic	Min	Тур ⁽¹⁾	Max	Units	Conditions	
40	Tt0H	T0CKI High Pulse Width - No Pre	escaler	0.5 Tcy + 20*	—		ns	
		- With P	rescaler	10*	_		ns	
41	Tt0L	T0CKI Low Pulse Width - No Pre	escaler	0.5 Tcy + 20*	_		ns	
		- With P	rescaler	10*	_		ns	
42	Tt0P	T0CKI Period		20 or <u>Tcy + 40</u> * N		_	ns	Whichever is greater. N = Prescale Value (1, 2, 4,, 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

NOTES:

14.0 ELECTRICAL CHARACTERISTICS - PIC16C54A

Absolute Maximum Ratings[†]

Ambient temperature under bias	–55°C to +125°C
Storage temperature	–65°C to +150°C
Voltage on VDD with respect to VSS	0 to +7.5V
Voltage on MCLR with respect to Vss	
Voltage on all other pins with respect to Vss	
Total power dissipation ⁽¹⁾	800 mW
Max. current out of Vss pin	150 mA
Max. current into Vod pin	100 mA
Max. current into an input pin (T0CKI only)	
Input clamp current, Iк (Vi < 0 or Vi > VDD)	
Output clamp current, IOK (VO < 0 or VO > VDD)	
Max. output current sunk by any I/O pin	25 mA
Max. output current sourced by any I/O pin	20 mA
Max. output current sourced by a single I/O port (PORTA or B)	50 mA
Max. output current sunk by a single I/O port (PORTA or B)	50 mA
Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - \sum IOH} + \sum {(VDD-VC	OH) X IOH} + $∑$ (VOL X IOL)

[†] NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 14-1:CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS
AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C54A-04	PIC16C54A-10	PIC16C54A-20	PIC16LC54A-04
RC	VDD: 3.0V to 6.25V IDD: 2.4 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 4 MHz max.	VDD: 3.0V to 6.25V IDD: 1.7 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 1.7 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 0.5 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.
хт	VDD: 3.0V to 6.25V IDD 2.4 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 4 MHz max.	VDD: 3.0V to 6.25V IDD: 1.7 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 1.7 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 0.5 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.
нѕ	N/A	VDD: 4.5V to 5.5V IDD: 8.0 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 10 MHz max.	 VDD: 4.5V to 5.5V IDD: 16 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 20 MHz max. 	Do not use in HS mode
LP	VDD: 3.0V to 6.25V IDD: 14 μA typ. at 32kHz, 3.0V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 200 kHz max.	Do not use in LP mode	Do not use in LP mode	VDD: 2.5V to 6.25V IDD: 27 μA max. at 32kHz, 2.5V WDT dis IPD: 4.0 μA max. at 2.5V WDT dis Freq: 200 kHz max.

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

OSC	PIC16C54A/JW	PIC16LV54A-02
RC	VDD: 3.0V to 6.25V IDD: 2.4 mA max. at 5.5V	VDD: 2.0V to 3.8V IDD: 0.5 mA typ. at 3.0V
	IPD: 4.0 μA max. at 3.0V WDT dis Freq: 4.0 MHz max.	IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 2.0 MHz max.
хт	VDD: 3.0V to 6.25V IDD 2.4 mA max. at 5.5V	VDD: 2.0V to 3.8V IDD: 0.5 mA typ. at 3.0V
	IPD: 4.0 μA max. at 3.0V WDT dis Freq: 4.0 MHz max.	IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 2.0 MHz max.
нѕ	VDD: 4.5V to 5.5V IDD: 8 mA max. at 5.5V	Do not use in
	IPD: 4.0 μA max. at 3.0V WDT dis Freq: 10 MHz max.	HS mode
LP	VDD: 2.5V to 6.25V IDD: 27 μA max. at 32kHz, 2.5V WDT dis	VDD: 2.0V to 3.8V IDD: 27 μA max. at 32kHz, 2.5V WDT dis
	IPD: 4.0 µA max. at 2.5V WDT dis Freq: 200 kHz max.	IPD: 4.0 μA max. at 2.5V WDT dis Freq: 200 kHz max.

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

14.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial) PIC16C54A-04I, 10I, 20I (Industrial)

DC Characteristics Power Supply Pins		$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ (commercial)} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ (industrial)} \end{array}$							
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions			
Supply Voltage XT, RC and LP options HS option	Vdd	3.0 4.5		6.25 5.5	V V				
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP mode			
VDD start voltage to ensure Power-On Reset	VPOR		Vss		V	See Section 7.4 for details on Power-on Reset			
VDD rise rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset			
Supply Current ⁽³⁾ XT and RC ⁽⁴⁾ options HS option LP option, Commercial LP option, Industrial	IDD		1.8 2.4 4.5 14 17	2.4 8.0 16 29 37	mA mA	Fosc = 4.0 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 20 MHz, VDD = $5.5V$ Fosc = 32 kHz, VDD = $3.0V$, WDT disabled Fosc = 32 kHz, VDD = $3.0V$, WDT disabled			
Power Down Current⁽⁵⁾ Commercial Industrial	IPD		4.0 0.25 5.0 0.3	12 4.0 14 5.0	μΑ μΑ μΑ μΑ	VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled			

* These parameters are characterized but not tested.

- Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
 - 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that
 - the device is in SLEEP mode.
 - 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
 - 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

14.2 DC Characteristics: PIC16C54A-04E, 10E, 20E (Extended)

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ (extended)							
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions		
Supply Voltage XT and RC options HS option	Vdd	3.5 4.5		5.5 5.5	V V			
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP mode		
VDD start voltage to ensure Power-On Reset	VPOR		Vss		V	See Section 7.4 for details on Power-on Reset		
VDD rise rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset		
Supply Current ⁽³⁾ XT and RC ⁽⁴⁾ options HS option	IDD		1.8 4.8 9.0	3.3 10 20	mA	Fosc = 4.0 MHz, VDD = 5.5V Fosc = 10 MHz, VDD = 5.5V Fosc = 20 MHz, VDD = 5.5V		
Power Down Current ⁽⁵⁾ XT and RC options	IPD		5.0 0.8	22 18	μΑ μΑ	VDD = 3.5V, WDT enabled VDD = 3.5V, WDT disabled		
HS option			4.0 0.25	22 18	μΑ μΑ	VDD = 3.5V, WDT enabled VDD = 3.5V, WDT disabled		

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
- 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to
 - Vss, TOCKI = VDD, \overline{MCLR} = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
- 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
- 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

14.3 DC Characteristics: PIC16LC54A-04 (Commercial) PIC16LC54A-04I (Industrial) PIC16LC54A-04E (Extended)

DC Characteristics Power Supply Pins	$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^\circ C \leq T A \leq +70^\circ C \mbox{ (commercial)} \\ -40^\circ C \leq T A \leq +85^\circ C \mbox{ (industrial)} \\ -40^\circ C \leq T A \leq +125^\circ C \mbox{ (extended)} \end{array}$						
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions	
Supply Voltage XT and RC options LP options	Vdd	3.0 2.5		6.25 6.25	V V		
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP mode	
VDD start voltage to ensure Power-On Reset	VPOR		Vss		V	See Section 7.4 for details on Power-on Reset	
VDD rise rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset	
Supply Current ⁽³⁾ XT and RC ⁽⁴⁾ options LP option, Commercial LP option, Industrial LP option, Extended	IDD		0.5 11 11 11	25 27 35 37	μA	Fosc = 4.0 MHz, VDD = $5.5V$ Fosc = 32 kHz, VDD = $2.5V$ WDT disabled Fosc = 32 kHz, VDD = $2.5V$ WDT disabled Fosc = 32 kHz, VDD = $2.5V$ WDT disabled	
Power Down Current ⁽⁵⁾ Commercial	IPD		2.5 0.25	12 4.0	μΑ μΑ	VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled	
Industrial Extended			2.5 0.25 2.5	14 5.0 15	μΑ μΑ μΑ	VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled VDD = 2.5V, WDT enabled	
			0.25	7.0	μA	VDD = 2.5V, WDT disabled	

* These parameters are characterized but not tested.

- Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
 - 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled toVss, TOCKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
 - 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
 - 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

14.4 <u>DC Characteristics:</u> <u>PIC16LV54A-02 (Commercial)</u> PIC16LV54A-02 (Industrial)

DC Characteristics Power Supply Pins		$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ (commercial)} \\ -20^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ (industrial)} \end{array}$						
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions		
Supply Voltage XT, RC and LP options	Vdd	2.0		3.8	v			
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP mode		
VDD start voltage to ensure Power-On Reset	VPOR		Vss		V	See Section 7.4 for details on Power-on Reset		
VDD rise rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset		
Supply Current ⁽³⁾ XT and RC ⁽⁴⁾ options LP option, Commercial LP option, Industrial	IDD		0.5 11 14	27 35	μA	Fosc = 2.0 MHz, VDD = $3.0V$ Fosc = 32 kHz, VDD = $2.5V$, WDT disabled Fosc = 32 kHz, VDD = $2.5V$, WDT disabled		
Power Down Current⁽⁵⁾⁽⁶⁾ Commercial Industrial	IPD		2.5 0.25 3.5 0.3	12 4.0 14 5.0	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled VDD = 2.5V, WDT enabled VDD = 2.5V, WDT enabled		

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
- 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are:
 - OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to V_{ss} , TOCKI = VDD, \overline{MCLR} = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
- 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
- 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.
- 6: The oscillator start-up time can be as much as 8 seconds for XT and LP oscillator selection, if the SLEEP mode is entered or during initial power-up.

14.5 <u>DC Characteristics:</u> <u>PIC16C54A-04, 10, 20, PIC16LC54A-04, PIC16LV54A-02 (Commercial)</u> <u>PIC16C54A-04I, 10I, 20I, PIC16LC54A-04I, PIC16LV54A-02I (Industrial)</u> <u>PIC16C54A-04E, 10E, 20E (Extended)</u>

		Standard O	perating C	onditions (u	nless c	otherwise specified)			
		Operating Te				°C (commercial)			
DC Characteristics		opolating to	mporataro						
All Pins Except		-40° C ≤ Ta ≤ +85°C (industrial) -20° C ≤ Ta ≤ +85°C (industrial - PIC16LV54A-02I)							
Power Supply Pins		$-20^{\circ}C \le TA \le +85^{\circ}C$ (industrial - PIC16LV54A-02I) -40^{\circ}C \le TA \le +125^{\circ}C (extended)							
Power Supply Fins									
		Section 14.3		range is de	escribed	I in Section 14.1, Section 14.2 and			
Characteristic	Sym	Min	Тур ⁽¹⁾	Max	Units	Conditions			
Input Low Voltage	VIL								
I/O ports		Vss		0.2 Vdd	V	Pin at hi-impedance			
MCLR (Schmitt Trigger)		Vss		0.15 VDD	V				
T0CKI (Schmitt Trigger)		Vss		0.15 VDD	v				
OSC1 (Schmitt Trigger)		Vss		0.15 VDD	v	RC option only ⁽⁴⁾			
OSC1 (Schink Higger)		VSS VSS		0.13 VDD	V	XT, HS and LP options			
		V 55		0.3 VDD	V				
Input High Voltage	Vін								
I/O ports		0.2 VDD+1V		Vdd	V	For all VDD ⁽⁵⁾			
		2.0		Vdd	V	4.0V < VDD ≤ 5.5V ⁽⁵⁾			
MCLR (Schmitt Trigger)		0.85 Vdd		Vdd	V				
T0CKI (Schmitt Trigger)		0.85 Vdd		Vdd	V				
OSC1 (Schmitt Trigger)		0.85 VDD		Vdd	V	RC option only ⁽⁴⁾			
OSC1		0.7 VDD		VDD	v	XT, HS and LP options			
Hysteresis of Schmitt Trigger inputs	VHYS	0.15Vdd*			V				
Input Leakage Current ⁽³⁾	lı∟					For VDD \leq 5.5V			
I/O ports		-1.0	0.5	+1.0	μA	$Vss \leq Vpin \leq Vdd$,			
			0.0		part	Pin at hi-impedance			
MCLR		-5.0		+5.0	μA	$V_{PIN} = V_{SS} + 0.25 V^{(2)}$			
MOER		-5.0	0.5	+3.0	μΑ	$V_{PIN} = V_{DD}^{(2)}$			
тоскі		-3.0		+3.0	· ·	V = V D C V V = V D C V V = V D C V			
			0.5	+3.0	μΑ				
OSC1		-3.0	0.5		μΑ	$Vss \leq VPIN \leq VDD,$			
						XT, HS and LP options			
Output Low Voltage	Vol								
I/O ports				0.6	V	IOL = 8.7 mA, VDD = 4.5V			
OSC2/CLKOUT				0.6	V	IOL = 1.6 mA, VDD = 4.5V,			
						RC option only			
Output High Voltage	Vон					-			
I/O ports ⁽³⁾		Vdd-0.7			V	ІОН = -5.4 mA, VDD = 4.5V			
OSC2/CLKOUT		VDD-0.7 VDD-0.7			V	IOH = -3.4 MA, VDD = 4.5 V IOH = -1.0 mA, VDD = 4.5 V,			
		VUU-0.7			v	RC option only			

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.
- 3: Negative current is defined as coming out of the pin.
- 4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.
- 5: The user may use the better of the two specifications.

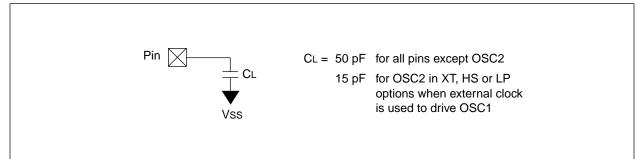
14.6 <u>Timing Parameter Symbology and Load Conditions</u>

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS

	1 I -			
2. TppS				
Т				
F	Frequency	Т	Time	
Lowerc	case subscripts (pp) and their meanings:			
рр				
2	to	mc	MCLR	
ck	CLKOUT	osc	oscillator	
су	cycle time	os	OSC1	
drt	device reset timer	tO	TOCKI	
io	I/O port	wdt	watchdog timer	
Upperc	case letters and their meanings:			
S				
F	Fall	P	Period	
н	High	R	Rise	
	Invalid (Hi-impedance)	V	Valid	
L _	Low	Z	Hi-impedance	

FIGURE 14-1: LOAD CONDITIONS - PIC16C54A



14.7 **Timing Diagrams and Specifications**

FIGURE 14-2: EXTERNAL CLOCK TIMING - PIC16C54A

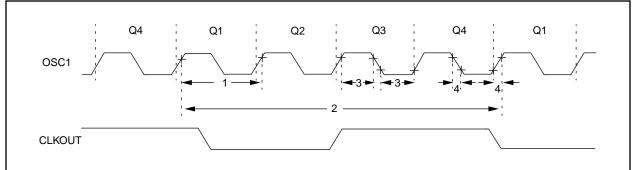


TABLE 14-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54A

AC Charac	cteristics								
Parameter No.	Sym	Characteristic	Min	Тур ⁽¹⁾	Max	Units	Conditions		
	Fosc	External CLKIN Frequency ⁽²⁾	DC	_	4.0	MHz	XT osc mode		
			DC	—	2.0	MHz	XT osc mode (PIC16LV54A)		
			DC	_	4.0	MHz	HS osc mode (04)		
			DC	—	10	MHz	HS osc mode (10)		
			DC	—	20	MHz	HS osc mode (20)		
			DC	_	200	kHz	LP osc mode		
		Oscillator Frequency ⁽²⁾	DC	_	4.0	MHz	RC osc mode		
			DC	—	2.0	MHz	RC osc mode (PIC16LV54A)		
			0.1	—	4.0	MHz	XT osc mode		
			0.1	—	2.0	MHz	XT osc mode (PIC16LV54A)		
			4	_	4.0	MHz	HS osc mode (04)		
			4	_	10	MHz	HS osc mode (10)		
			4	_	20	MHz	HS osc mode (20)		
			5	_	200	kHz	LP osc mode		

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (Tcy) equals four times the input oscillator time base period.

AC Chara	cteristics	$\begin{array}{lll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \ (commercial) \\ & -40^{\circ}C \leq TA \leq +85^{\circ}C \ (industrial) \\ & -20^{\circ}C \leq TA \leq +85^{\circ}C \ (industrial - PIC16LV54A-02I) \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \ (extended) \\ \mbox{Operating Voltage VDD range is described in Section 14.1, Section 14.2 and Section 14.3.} \end{array}$							
Parameter No.	Sym	Characteristic	Min	Тур ⁽¹⁾	Max	Units	Conditions		
1	Tosc	External CLKIN Period ⁽²⁾	250	_	_	ns	XT osc mode		
			500	_	_	ns	XT osc mode (PIC16LV54A)		
			250	_	_	ns	HS osc mode (04)		
			100	_	_	ns	HS osc mode (10)		
			50	_	_	ns	HS osc mode (20)		
			5.0	_	_	μs	LP osc mode		
		Oscillator Period ⁽²⁾	250	_	_	ns	RC osc mode		
			500	_	_	ns	RC osc mode (PIC16LV54A)		
			250	_	10,000	ns	XT osc mode		
			500	_	_	ns	XT osc mode (PIC16LV54A)		
			250	_	250	ns	HS osc mode (04)		
			100	_	250	ns	HS osc mode (10)		
			50	_	250	ns	HS osc mode (20)		
			5.0	_	200	μs	LP osc mode		
2	Тсү	Instruction Cycle Time ⁽³⁾		4/Fosc	—	_			
3	TosL, TosH	Clock in (OSC1) Low or High Time	85*	_	_	ns	XT oscillator		
			20*	_	_	ns	HS oscillator		
			2.0*	_	_	μs	LP oscillator		
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	_		25*	ns	XT oscillator		
			_	_	25*	ns	HS oscillator		
			_	_	50*	ns	LP oscillator		

TABLE 14-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54A (CON'T)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (Tcr) equals four times the input oscillator time base period.

FIGURE 14-3: CLKOUT AND I/O TIMING - PIC16C54A

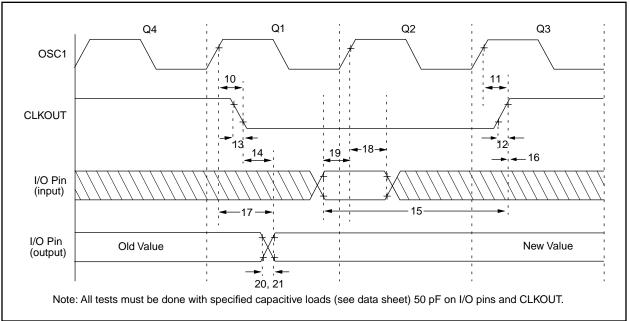


TABLE 14-3:	CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54A
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AC Chara	cteristics	$\begin{array}{llllllllllllllllllllllllllllllllllll$				
Parameter No.	Sym	Characteristic	Min	Тур ⁽¹⁾	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽²⁾	_	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽²⁾	_	15	30**	ns
12	TckR	CLKOUT rise time ⁽²⁾	_	5.0	15**	ns
13	TckF	CLKOUT fall time ⁽²⁾	_	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽²⁾	_	_	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑ ⁽²⁾	0.25 TCY+30*	_	_	ns
16	TckH2iol	Port in hold after CLKOUT↑ ⁽²⁾	0*	_	_	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid ⁽³⁾	—	_	100*	ns
18	TosH2iol	OSC1 [↑] (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	-	_	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	-		ns
20	TioR	Port output rise time ⁽³⁾	_	10	25**	ns
21	TioF	Port output fall time ⁽³⁾	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

3: See Figure 14-1 for loading conditions.

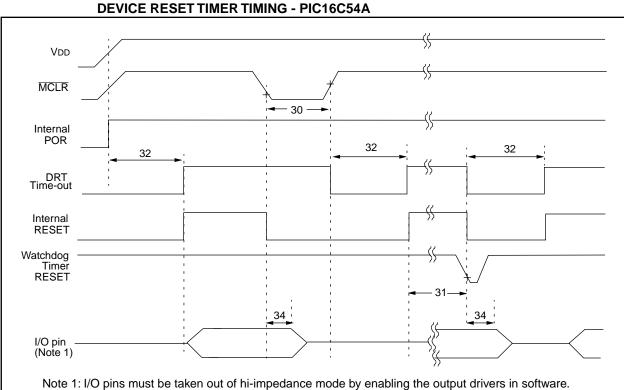


FIGURE 14-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54A

TABLE 14-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54A

AC Charac	teristics	Standard Operating Conditions (unless otherwise specified)								
		Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ (commercial)								
		-40	°C ≤ TA	≤ +85°0	C (indus	strial)				
		-20	°C ≤ TA	≤ +85°0	C (indus	strial - P	IC16LV54A-02I)			
		-40	°C ≤ TA	≤ +125	°C (exte	ended)	,			
		Operating Voltage VDD range is					ction 14.2 and Section 14.3.			
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions			
30	TmcL	MCLR Pulse Width (low)	100* 1μs			ns	VDD = 5.0V VDD = 5.0V (PIC16LV54A only)			
31 Twdt		Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)			
32	Tdrt	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)			
34	Tioz I/O Hi-impedance from MCLR		_	_	100* 1μs	ns	(PIC16LV54A only)			

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 14-5: TIMER0 CLOCK TIMINGS - PIC16C54A

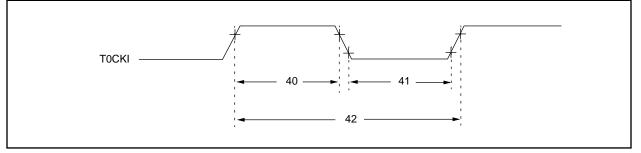


TABLE 14-5: **TIMER0 CLOCK REQUIREMENTS - PIC16C54A**

-40°C -20°C -40°C Operating Voltage VDD range is Section 14.3.				≦ TA ≤ + ≤ TA ≤ + ≤ TA ≤ + ≤ TA ≤ + ≤ TA ≤ +	-70°C -85°C -85°C -85°C -125°((comme (industi (industi C (exter	ercial) rial) rial - PIC16LV54A-02I) nded)
Parameter No.	Sym	Characteristic	Min	Тур ⁽¹⁾	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	-	—	ns	
		- With Prescaler	10*	-	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	-	—	ns	
		- With Prescaler	10*	_	—	ns	
42	Tt0P	T0CKI Period	20 or <u>Tcy + 40</u> * N		_	ns	Whichever is greater. N = Prescale Value (1, 2, 4,, 256)

 * These parameters are characterized but not tested.
 Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

NOTES:

15.0 ELECTRICAL CHARACTERISTICS - PIC16CR57B

Absolute Maximum Ratings†

5.	
Ambient Temperature under bias	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on VDD with respect to Vss	0 to +7.5V
Voltage on MCLR with respect to Vss	0 to +14V
Voltage on all other pins with respect to Vss	0.6V to (VDD + 0.6V)
Total Power Dissipation ⁽¹⁾	
Max. Current out of Vss pin	150 mA
Max. Current into VDD pin	
Max. Current into an input pin (T0CKI only)	±500 μA
Input Clamp Current, Iк (VI < 0 or VI > VDD)	±20 mA
Output Clamp Current, IOK (VO < 0 or VO > VDD)	±20 mA
Max. Output Current sunk by any I/O pin	25 mA
Max. Output Current sourced by any I/O pin	20 mA
Max. Output Current sourced by a single I/O port (PORTA, B or C)	50 mA
Max. Output Current sunk by a single I/O port (PORTA, B or C)	50 mA
Note 1: Power Dissipation is calculated as follows: PDIS = VDD x {IDD - \sum IOH} + \sum	$\Sigma \{(VDD-VOH) \times IOH\} + \Sigma(VOL \times IOL)$

[†]NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 15-1:CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS
AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16CR57B-04	PIC16CR57B-10	PIC16CR57B-20	PIC16LCR57B-04
RC	VDD: 3.0V to 6.25V IDD: 2.5 mA max at 5.5V IPD: 4.0 μA max at 3.0V, WDT dis Freq: 4.0 MHz max	N/A	N/A	N/A
ХТ	VDD: 3.0V to 6.25V IDD: 2.5 mA max at 5.5V IPD: 4.0 μA max at 3.0V, WDT dis Freq: 4.0 MHz max	N/A	N/A	N/A
HS	N/A	VDD: 4.5V to 5.5V IDD: 10 mA max at 5.5V IPD: 4.0 μA max at 3.0V, WDT dis Freq: 10 MHz max	VDD: 4.5V to 5.5V IDD: 20 mA max at 5.5V IPD: 4.0 μA max at 3.0V, WDT dis Freq: 20 MHz max	N/A
LP	N/A	N/A	N/A	 VDD: 2.5V to 6.25V IDD: 32 μA max at 32 kHz, 2.5V IPD: 4.0 μA max at 2.5V, WDT dis Freq: 200 kHz max

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

15.1 DC Characteristics: PIC16CR57B-04, 10, 20 (Commercial) PIC16CR57B-04I, 10I, 20I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \leq TA \leq +70^{\circ}C$ (commercial) $-40^{\circ}C \leq TA \leq +85^{\circ}C$ (industrial)						
Characteristic	Sym	Min	Typ ⁽¹⁾	Мах	Units	Conditions		
Supply Voltage RC and XT options HS option	Vdd	3.0 4.5		6.25 5.5	V V			
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP mode		
VDD Start Voltage to ensure Power-on Reset	VPOR		Vss		V	See Section 7.4 for details on Power-on Reset		
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset		
Supply Current ⁽³⁾ RC ⁽⁴⁾ and XT options HS option	IDD		1.9 2.5 4.7	2.5 8.0 17	mA mA mA	Fosc = 4 MHz, Vdd = 5.5V Fosc = 10 MHz, Vdd = 5.5V Fosc = 20 MHz, Vdd = 5.5V		
Power-Down Current ⁽⁵⁾ Commercial	IPD		4.0 0.25	12 4.0	μA μA	VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled		
Industrial			4.0 0.25	14 5.0	μΑ μΑ	VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled		

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

15.2 DC Characteristics: PIC16CR57B-04E, 10E, 20E (Extended)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ (extended)						
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions		
Supply Voltage	Vdd							
RC and XT options		3.25		6.0	V			
HS options		4.5		5.5	V			
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP mode		
VDD Start Voltage to ensure Power-on Reset	VPOR		Vss		V	See Section 7.4 for details on Power-on Reset		
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset		
Supply Current ⁽³⁾	IDD							
RC ⁽⁴⁾ and XT options			1.9	3.3	mA	FOSC = 4 MHz, VDD = 5.5V		
HS option			4.8	10	mA	Fosc = 10 MHz, VDD = 5.5V		
			9.0	20	mA	Fosc = 20 MHz, VDD = 5.5V		
Power-Down Current ⁽⁵⁾	IPD							
			5.0	22	μA	VDD = 3.25V, WDT enabled		
			0.8	18	μA	VDD = 3.25V, WDT disabled		

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
- 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
- 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
- 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

15.3 <u>DC Characteristics:</u> <u>PIC16LCR57B-04 (Commercial)</u> <u>PIC16LCR57B-04I (Industrial)</u>

DC Characteristics Power Supply Pins			ard Oper ing Temp	-	0°	s (unless otherwise specified) $C \le TA \le +70^{\circ}C$ (commercial) $C \le TA \le +85^{\circ}C$ (industrial)
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions
Supply Voltage	Vdd	2.5		6.25	V	LP option
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR		Vss		V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset
Supply Current ⁽³⁾ Commercial Industrial	IDD		12 15	28 37	μΑ μΑ	Fosc = 32 kHz, VDD = 2.5V, WDT disabled Fosc = 32 kHz, VDD = 2.5V, WDT disabled
Power-Down Current⁽⁵⁾ Commercial Industrial	IPD		3.5 0.2 3.5 0.2	12 4.0 14 5.0	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled

- Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
 - 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to V_{ss} , T0CKI = VDD, $\overline{MCLR} = VDD$; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
 - 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
 - 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

15.4 DC Characteristics: PIC16CR57B-04, 10, 20, PIC16LCR57B-04 (Commercial) PIC16CR57B-04I, 10I, 20I, PIC16LCR57B-04I (Industrial)

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \leq TA \leq +70^{\circ}C$ (commercial) $-40^{\circ}C \leq TA \leq +85^{\circ}C$ (industrial)Operating Voltage VDD range is described in Section 15.1 and Section 15.3.								
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions				
	-		17P	Max	Units					
Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	VIL	Vss Vss Vss Vss Vss		0.2 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V	Pin at hi-impedance RC option only ⁽⁴⁾ XT, HS and LP options				
Input High Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	Vih	0.45 VDD 2.0 0.36 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD		VDD VDD VDD VDD VDD VDD VDD	V V V V V V	For all VDD ⁽⁵⁾ $4.0V < VDD \le 5.5V^{(5)}$ VDD > 5.5V RC option only ⁽⁴⁾ XT, HS and LP options				
Hysteresis of Schmitt Trigger inputs	VHYS	0.15Vdd*			V					
Input Leakage Current ⁽³⁾ I/O ports	lı∟	-1.0 -5.0		+1.0	μA	For VDD \leq 5.5V VSS \leq VPIN \leq VDD, Pin at hi-impedance VPIN = VSS + 0.25V ⁽²⁾				
TOCKI OSC1		-3.0 -3.0 -3.0	0.5 0.5 0.5	+5.0 +3.0 +3.0	μΑ μΑ μΑ μΑ	$V_{PIN} = V_{DD}(2)$ $V_{SS} \le V_{PIN} \le V_{DD}$ $V_{SS} \le V_{PIN} \le V_{DD}$ $X_{T}, HS and LP options$				
Output Low Voltage I/O ports OSC2/CLKOUT	Vol			0.6 0.6	V V	IOL = 8.7 mA, VDD = 4.5 V IOL = 1.6 mA, VDD = 4.5 V, RC option only				
Output High Voltage ⁽³⁾ I/O ports OSC2/CLKOUT	Vон	Vdd -0.7 Vdd -0.7			V V	IOH = -5.4 mA, VDD = 4.5V IOH = -1.0 mA, VDD = 4.5V, RC option only				

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

- 4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.
- 5: The user may use the better of the two specifications.

15.5 DC Characteristics: PIC16CR57B-04E, 10E, 20E (Extended)

DC Characteristics All Pins Except Power Supply Pins		Operating Te	emperati	ire -	-40°C ≤ 1	otherwise specified) Fa ≤ +125°C n Section 15.2.
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions
Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	VIL	Vss Vss Vss Vss Vss		0.2 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V	Pin at hi-impedance RC option only ⁽⁴⁾ XT, HS and LP options
Input High Voltage I/O ports MCLR (Schmitt Trigger) TOCKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	VIH	0.45 VDD 2.0 0.36 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD		VDD VDD VDD VDD VDD VDD VDD	V V V V V V	For all VDD ⁽⁵⁾ $4.0V < VDD \le 5.5V^{(5)}$ VDD > 5.5V RC option only ⁽⁴⁾ XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	VHYS	0.15Vdd*			V	
Input Leakage Current ⁽³⁾ I/O ports MCLR TOCKI OSC1	IIL.	-1.0 -5.0 -3.0 -3.0	0.5 0.5 0.5	+1.0 +5.0 +3.0 +3.0	μΑ μΑ μΑ μΑ	$\begin{array}{l} \mbox{For VDD} \leq \mbox{5.5V} \\ \mbox{Vss} \leq \mbox{VPIN} \leq \mbox{VDD}, \\ \mbox{Pin at hi-impedance} \\ \mbox{VPIN} = \mbox{Vss} + 0.25 \ \mbox{V}^{(2)} \\ \mbox{VPIN} = \mbox{VDD}^{(2)} \\ \mbox{Vss} \leq \mbox{VPIN} \leq \mbox{VDD} \\ \mbox{Vss} \leq \mbox{VPIN} \leq \mbox{VDD} \\ \mbox{Vss} \leq \mbox{VPIN} \leq \mbox{VDD}, \\ \mbox{XT, HS and LP options} \end{array}$
Output Low Voltage I/O ports OSC2/CLKOUT	Vol			0.6 0.6	V V	IOL = 8.7 mA, VDD = $4.5V$ IOL = 1.6 mA, VDD = $4.5V$, RC option only
Output High Voltage ⁽³⁾ I/O ports OSC2/CLKOUT	Vон	Vdd0.7 Vdd0.7			V V	IOH = -5.4 mA, $VDD = 4.5VIOH = -1.0$ mA, $VDD = 4.5V$, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

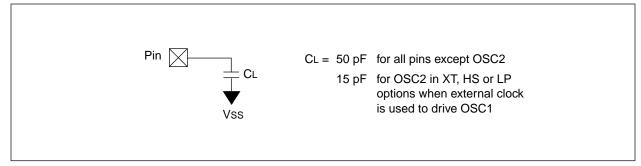
15.6 <u>Timing Parameter Symbology and Load Conditions</u>

The timing parameter symbols have been created following one of the following formats:

- 1. TppS2ppS
- 2. TppS

2. 1000			
т			
F	Frequency	Т	Time
Lowerc	case subscripts (pp) and their meanings:		
рр			
2	to	mc	MCLR
ck	CLKOUT	osc	oscillator
су	cycle time	os	OSC1
drt	device reset timer	tO	TOCKI
io	I/O port	wdt	watchdog timer
Upperc	case letters and their meanings:		
S			
F	Fall	Р	Period
Н	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 15-1: LOAD CONDITIONS



15.7 **Timing Diagrams and Specifications**

FIGURE 15-2: EXTERNAL CLOCK TIMING - PIC16CR57B

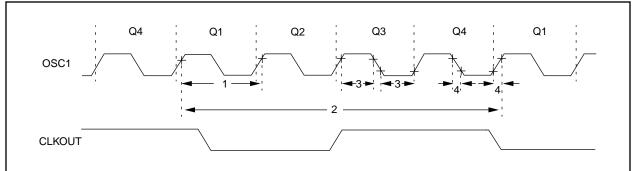


TABLE 15-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR57B

		$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ (commercial)} \\ & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ (industrial)} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ (extended)} \\ \mbox{Operating Voltage VDD range is described in Section 15.1, Section 15.2 and Section 15.3.} \end{array}$								
Parameter No.	Sym	Characteristic	Min	Тур ⁽¹⁾	Max	Units	Conditions			
	Fosc	External CLKIN Frequency ⁽²⁾	DC	_	4.0	MHz	XT osc mode			
			DC	—	4.0	MHz	HS osc mode (04)			
			DC	—	10	MHz	HS osc mode (10)			
			DC	—	20	MHz	HS osc mode (20)			
			DC	—	200	kHz	LP osc mode			
		Oscillator Frequency ⁽²⁾	DC		4.0	MHz	RC osc mode			
			0.1	—	4.0	MHz	XT osc mode			
			4.0	—	4.0	MHz	HS osc mode (04)			
			4.0	—	10	MHz	HS osc mode (10)			
		4.0 — 20 MHz HS osc mode (20)								
			5.0	—	200	kHz	LP osc mode			

These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

TABLE 15-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR57B (CON'T)

AC Chara	cteristics	$\begin{array}{l} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ (commercial)} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ (industrial)} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ (extended)} \\ \mbox{Operating Voltage VDD range is described in Section 15.1, Section 15.2 and Section 15.3.} \end{array}$								
Parameter No.	Sym	Characteristic	Characteristic Min Typ ⁽¹⁾ Max Units Condition							
1	Tosc	External CLKIN Period ⁽²⁾	250	_	_	ns	XT osc mode			
			250	_	_	ns	HS osc mode (04)			
			100	_	_	ns	HS osc mode (10)			
			50	_	_	ns	HS osc mode (20)			
			5.0	_	—	μs	LP osc mode			
		Oscillator Period ⁽²⁾	250	_	—	ns	RC osc mode			
			250	_	10,000	ns	XT osc mode			
			250	_	250	ns	HS osc mode (04)			
			100	-	250	ns	HS osc mode (10)			
			50	-	250	ns	HS osc mode (20)			
			5.0	_	200	μs	LP osc mode			
2	Тсү	Instruction Cycle Time ⁽³⁾	—	4/Fosc	—					
3	TosL, TosH	Clock in (OSC1) Low or High Time	85*	_	—	ns	XT oscillator			
			20*	_		ns	HS oscillator			
			2.0*	_	_	μs	LP oscillator			
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	_	_	25*	ns	XT oscillator			
			_	_	25*	ns	HS oscillator			
				_	50*	ns	LP oscillator			

* These parameters are characterized but not tested.

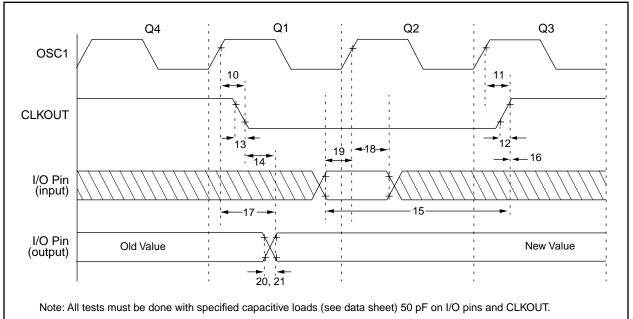
Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (Tcy) equals four times the input oscillator time base period.

FIGURE 15-3: CLKOUT AND I/O TIMING - PIC16CR57B



AC Chara	cteristics	-40°C ≤ TA ≤	+70°C (comme +85°C (industri +125°C (extend	rcial) al) ded)		5.2 and
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽²⁾	_	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽²⁾	_	15	30**	ns
12	TckR	CLKOUT rise time ⁽²⁾	_	5.0	15**	ns
13	TckF	CLKOUT fall time ⁽²⁾	_	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽²⁾	—	_	40**	ns
15	TioV2ckH	Port in valid before CLKOUT ⁽²⁾	0.25 TCY+30*	_	_	ns
16	TckH2iol	Port in hold after CLKOUT ⁽²⁾	0*	_	_	ns
17	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port out valid ⁽³⁾	_	_	100*	ns
18	TosH2iol	OSC1 [↑] (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	-	_	ns
19	TioV2osH	Port input valid to OSC1 [↑] (I/O in setup time)	TBD	-	_	ns
20	TioR	Port output rise time ⁽³⁾	_	10	25**	ns
21	TioF	Port output fall time ⁽³⁾	_	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

3: See Figure 15-1 for loading conditions.

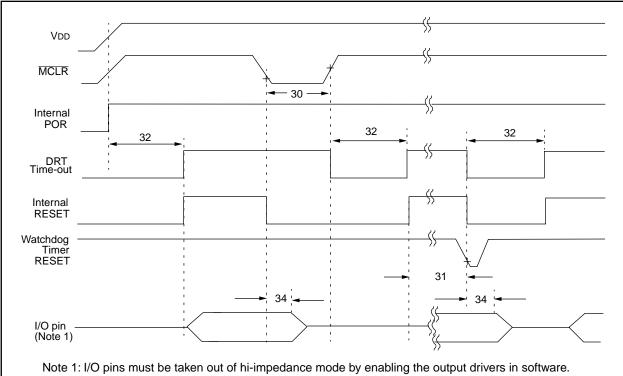


FIGURE 15-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16CR57B

TABLE 15-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16CR57B

AC Charac	teristics	Operating Temperature $0^{\circ}C \le -40^{\circ}C \le -40^{\circ}C \le -40^{\circ}C \le 0^{\circ}C \le $	Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ (commercial) $-40^{\circ}C \le TA \le +85^{\circ}C$ (industrial) $-40^{\circ}C \le TA \le +125^{\circ}C$ (extended)Operating Voltage VDD range is described in Section 15.1, Section 15.2 and Section 15.3.							
Parameter No.	Sym	Characteristic	characteristic Min Typ ⁽¹⁾ Max							
30	TmcL	MCLR Pulse Width (low)	1.0*	_		μs	VDD = 5.0V			
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)			
32	Tdrt	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)			
34	Tioz	I/O Hi-impedance from MCLR Low		_	1.0*	μs				

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 15-5: TIMER0 CLOCK TIMINGS - PIC16CR57B

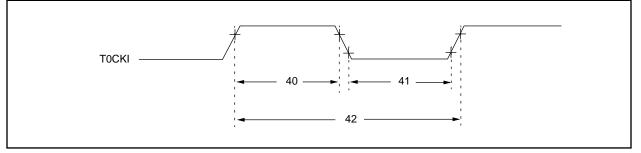


TABLE 15-5:TIMER0 CLOCK REQUIREMENTS - PIC16CR57B

AC	Charao	cteristics	Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ (commercial) $-40^{\circ}C \le TA \le +85^{\circ}C$ (industrial) $-40^{\circ}C \le TA \le +125^{\circ}C$ (extended)Operating Voltage VDD range is described in Section 15.1, Section 15Section 15.3.					
Parameter No.	Sym	Characteristic	Min	Тур ⁽¹⁾	Мах	Units	Conditions	
40	Tt0H	T0CKI High Pulse V	Vidth - No Prescaler	0.5 TCY + 20*	—	—	ns	
			- With Prescaler	10*	_	_	ns	
41	Tt0L	T0CKI Low Pulse V	/idth - No Prescaler	0.5 TCY + 20*	_	_	ns	
			- With Prescaler	10*	—	_	ns	
42	Tt0P	T0CKI Period		20 or <u>TCY + 40</u> * N		_	ns	Whichever is greater. N = Prescale Value (1, 2, 4,, 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

NOTES:

16.0 ELECTRICAL CHARACTERISTICS - PIC16C58A

Absolute Maximum Ratings[†]

Ambient Temperature under bias	55°C to +125°C
Ambient Temperature under bias Storage Temperature	–65°C to +150°C
Voltage on VDD with respect to Vss	
Voltage on MCLR with respect to Vss	0 to +14V
Voltage on all other pins with respect to Vss	
Total Power Dissipation ⁽¹⁾	800 mW
Max. Current out of Vss pin	150 mA
Max. Current into VDD pin	100 mA
Max. Current into an input pin (T0CKI only)	±500 μA
Input Clamp Current, Iк (VI < 0 or VI > VDD)	±20 mA
Output Clamp Current, IOK (VO < 0 or VO > VDD)	±20 mA
Max. Output Current sunk by any I/O pin	
Max. Output Current sourced by any I/O pin	20 mA
Max. Output Current sourced by a single I/O port (PORTA or B)	50 mA
Max. Output Current sunk by a single I/O port (PORTA or B)	50 mA
Note 1: Power Dissipation is calculated as follows: Pdis = VDD x {IDD - \sum IOH} + \sum {(VDD-VO	(VOL X IOH) + Σ (VOL X IOL)

[†] NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 16-1:CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS
AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C58A-04	PIC16C58A-10	PIC16C58A-20	PIC16LC58A-04
RC	VDD: 3.0V to 6.25V IDD: 2.5 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 1.8 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 1.8 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 0.5 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.
хт	VDD: 3.0V to 6.25V IDD 2.5 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 1.8 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 1.8 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 0.5 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.
HS	N/A	VDD: 4.5V to 5.5V IDD: 8.0 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 10 MHz max.	VDD: 4.5V to 5.5V IDD: 17 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 20 MHz max.	Do not use in HS mode
LP	VDD: 3.0V to 6.25V IDD: 15 μA typ. at 32kHz, 3.0V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 200 kHz max.	Do not use in LP mode	Do not use in LP mode	VDD: 2.5V to 6.25V IDD: 28 μA max. at 32kHz, 2.5V WDT dis IPD: 4.0 μA max. at 2.5V WDT dis Freq: 200 kHz max.

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

OSC	PIC16C58A/JW	PIC16LV58A-02
RC	VDD: 3.0V to 6.25V IDD: 2.5 mA max. at 5.5V	VDD: 2.0V to 3.8V IDD: 0.5 mA typ. at 3.0V
	IPD: 4.0 μA max. at 3.0V WDT dis Freq: 4.0 MHz max.	IPD: 0.25 µA typ. at 3.0V WDT dis Freq: 2.0 MHz max.
	VDD: 3.0V to 6.25V IDD 2.5 mA max. at 5.5V	VDD: 2.0V to 3.8V IDD: 0.5 mA typ. at 3.0V
ХТ	IPD: 4.0 μA max. at 3.0V WDT dis Freq: 4.0 MHz max.	IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 2.0 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 17 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 20 MHz max.	Do not use in HS mode
LP	VDD: 2.5V to 6.25V IDD: 28 μA max. at 32kHz, 2.5V WDT dis IPD: 4.0 μA max. at 2.5V WDT dis	VDD: 2.0V to 3.8V IDD: 27 μA max. at 32kHz, 2.5V WDT dis IPD: 4.0 μA max. at 2.5V WDT dis
	Freq: 200 kHz max.	Freq: 200 kHz max.

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

16.1 DC Characteristics: PIC16C58A-04, 10, 20 (Commercial) PIC16C58A-04I, 10I, 20I (Industrial)

DC Characteristics Power Supply Pins		$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ (commercial)} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ (industrial)} \end{array}$							
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions			
Supply Voltage XT, RC and LP options HS option	Vdd	3.0 4.5		6.25 5.5	V V				
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP mode			
VDD start voltage to ensure Power-On Reset	VPOR		Vss		V	See Section 7.4 for details on Power-on Reset			
VDD rise rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset			
Supply Current ⁽³⁾ XT and RC ⁽⁴⁾ options HS option LP option, Commercial LP option, Industrial	IDD		1.9 2.5 4.7 15 18	2.5 8.0 17 31 39	mA mA	Fosc = 4.0 MHz, VDD = $5.5V$ Fosc = 10 MHz, VDD = $5.5V$ Fosc = 20 MHz, VDD = $5.5V$ Fosc = 32 kHz, VDD = $3.0V$, WDT disabled Fosc = 32 kHz, VDD = $3.0V$, WDT disabled			
Power Down Current ⁽⁵⁾ Commercial Industrial	IPD		4.0 0.25 5.0 0.3	12 4.0 14 5.0	μΑ μΑ	VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled VDD = 3.0V, WDT disabled VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled			

- Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
 - 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, TOCKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that
 - the device is in SLEEP mode.
 - 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
 - 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

16.2 DC Characteristics: PIC16C58A-04E, 10E, 20E (Extended)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ (extended)							
Characteristic Sym			Typ ⁽¹⁾	Max	Units	Conditions			
Supply Voltage XT and RC options HS option	Vdd	3.5 4.5		5.5 5.5	V V				
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP mode			
VDD start voltage to ensure Power-On Reset	VPOR		Vss		V	See Section 7.4 for details on Power-on Reset			
VDD rise rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset			
Supply Current ⁽³⁾ XT and RC ⁽⁴⁾ options HS option	IDD		1.9 4.8 9.0	3.3 10 20	mA	Fosc = 4.0 MHz, VDD = 5.5V Fosc = 10 MHz, VDD = 5.5V Fosc = 20 MHz, VDD = 5.5V			
Power Down Current⁽⁵⁾ XT and RC options HS option	IPD		5.0 0.8 4.0 0.25	22 18 22 18	μΑ μΑ μΑ μΑ	VDD = 3.5V, WDT enabled VDD = 3.5V, WDT disabled VDD = 3.5V, WDT enabled VDD = 3.5V, WDT disabled			

- Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
 - 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are:
 - OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to
 - Vss, T0CKI = VDD, \overline{MCLR} = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
 - 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
 - 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

16.3 <u>DC Characteristics:</u> <u>PIC16LC58A-04 (Commercial)</u> <u>PIC16LC58A-04I (Industrial)</u> <u>PIC16LC58A-04 (Extended)</u>

DC Characteristics Power Supply PinsStandard Operating Conditions (unless otherwise specified) Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ (commercial) $-40^{\circ}C \le TA \le +85^{\circ}C$ (industrial) $-40^{\circ}C \le TA \le +125^{\circ}C$ (extended)										
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions				
Supply Voltage XT and RC options LP options	Vdd	3.0 2.5		6.25 6.25	V V					
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP mode				
VDD start voltage to ensure Power-On Reset	VPOR		Vss		V	See Section 7.4 for details on Power-on Reset				
VDD rise rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset				
Supply Current ⁽³⁾ XT and RC ⁽⁴⁾ options LP option, Commercial LP option, Industrial LP option, Extended	IDD		0.5 12 12 12	2.5 27 35 37	μA	Fosc = 4.0 MHz, VDD = $5.5V$ Fosc = 32 kHz, VDD = $2.5V$ WDT disabled Fosc = 32 kHz, VDD = $2.5V$ WDT disabled Fosc = 32 kHz, VDD = $2.5V$ WDT disabled				
Power Down Current ⁽⁵⁾ Commercial	IPD		2.5 0.25	12 4.0	μΑ μΑ	VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled				
Industrial Extended			2.5 0.25 2.5 0.25	14 5.0 15 7.0	•	VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled				

- Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
 - 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to
 - V_{ss} , T0CKI = VDD, \overline{MCLR} = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
 - 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
 - 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

16.4 <u>DC Characteristics:</u> <u>PIC16LV58A-02 (Commercial)</u> PIC16LV58A-02 (Industrial)

DC Characteristics Power Supply Pins		$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ (commercial)} \\ -20^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ (industrial)} \end{array}$							
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions			
Supply Voltage XT, RC and LP options	Vdd	2.0		3.8	V				
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP mode			
VDD start voltage to ensure Power-On Reset	VPOR		Vss		V	See section on Power-On Reset for details			
VDD rise rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See section on Power-On Reset for details			
Supply Current ⁽³⁾ XT and RC ⁽⁴⁾ options LP option, Commercial LP option, Industrial	IDD		0.5 11 14	1.8 27 35		Fosc = 2.0 MHz, VDD = $3.0V$ Fosc = 32 kHz, VDD = $2.5V$, WDT disabled Fosc = 32 kHz, VDD = $2.5V$, WDT disabled			
Power Down Current⁽⁵⁾⁽⁶⁾ Commercial Industrial	IPD		2.5 0.25 2.5 0.25	12 4.0 14 5.0	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled			

- Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
 - 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are:
 - OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to V_{ss} , T0CKI = VDD, \overline{MCLR} = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
 - 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
 - 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.
 - 6: The oscillator start-up time can be as much as 8 seconds for XT and LP oscillator selection, if the SLEEP mode is entered or during initial power-up.

16.5 <u>DC Characteristics:</u> <u>PIC16C58A-04, 10, 20, PIC16LC58A-04, PIC16LV58A-02 (Commercial)</u> <u>PIC16C58A-04I, 10I, 20I, PIC16LC58A-04I, PIC16LV58A-02I (Industrial)</u> <u>PIC16C58A-04E, 10E, 20E (Extended)</u>

		Standard O	perating C	onditions (u	nless c	otherwise specified)					
		Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ (commercial)									
DC Characteristics		opolating it	mporataro	$-40^{\circ}C \le TA \le +85^{\circ}C$ (industrial)							
All Pins Except		$-20^{\circ}C \le TA \le +85^{\circ}C$ (industrial) $-20^{\circ}C \le TA \le +85^{\circ}C$ (industrial - PIC16LV58A)									
Power Supply Pins											
Power Supply Pills		$-40^{\circ}C \le TA \le +125^{\circ}C$ (extended)									
		Operating Voltage VDD range is described in Section 16.1, Section 16.2 an Section 16.3.									
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions					
Input Low Voltage	VIL										
I/O ports		Vss		0.2 VDD	V	Pin at hi-impedance					
MCLR (Schmitt Trigger)		Vss		0.15 VDD	V						
T0CKI (Schmitt Trigger)		Vss		0.15 VDD	V						
OSC1 (Schmitt Trigger)		Vss		0.15 VDD	V	RC option only ⁽⁴⁾					
OSC1		Vss		0.3 VDD	v	XT, HS and LP options					
Input High Voltage	Viн	100		0.0 100							
I/O ports	VIH	0.2 VDD+1V		Vdd	V	For all VDD ⁽⁵⁾					
1/O ports					1						
		2.0		Vdd	V	$4.0V < VDD \le 5.5V^{(5)}$					
MCLR (Schmitt Trigger)		0.85 VDD		Vdd	V						
T0CKI (Schmitt Trigger)		0.85 VDD		Vdd	V	(4)					
OSC1 (Schmitt Trigger)		0.85 Vdd		Vdd	V	RC option only ⁽⁴⁾					
OSC1		0.7 Vdd		Vdd	V	XT, HS and LP options					
Hysteresis of Schmitt Trigger inputs	VHYS	0.15Vdd*			V						
Input Leakage Current ⁽³⁾	lı.					For VDD \leq 5.5V					
I/O ports		-1.0	0.5	+1.0	μA	$Vss \leq VPIN \leq VDD,$					
						Pin at hi-impedance					
MCLR		-5.0			μA	$V_{PIN} = V_{SS} + 0.25 V^{(2)}$					
MOEIX		0.0	0.5	+5.0	μΑ	$V_{\text{PIN}} = V_{\text{DD}}^{(2)}$					
тоскі		-3.0	0.5	+3.0	μΑ	$Vss \le Vpin \le Vdd$					
OSC1		-3.0	0.5	+3.0	μΑ	$V_{SS} \leq V_{PIN} \leq V_{DD}$					
0001		-3.0	0.5	+3.0	μΛ	XT, HS and LP options					
Output Low Voltage	Vol										
I/O ports				0.6	V	IOL = 8.7 mA, VDD = 4.5V					
OSC2/CLKOUT				0.6	v	IOL = 1.6 mA, VDD = 4.5 V,					
				0.0		RC option only					
Output High Voltage	Vон										
I/O ports ⁽³⁾		VDD-0.7			V	ІОН = -5.4 mA, VDD = 4.5V					
OSC2/CLKOUT		VDD-0.7			v	IOH = -1.0 mA, VDD = 4.5 V,					
						RC option only					
					1						

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- 2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.
- 3: Negative current is defined as coming out of the pin.
- 4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.
- 5: The user may use the better of the two specifications.

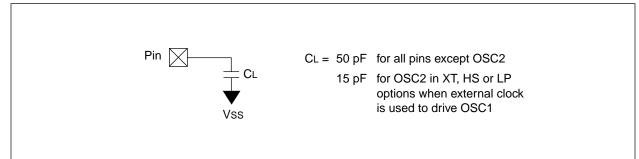
16.6 <u>Timing Parameter Symbology and Load Conditions</u>

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS

	FF -		
2. TppS			
Т			
F	Frequency	Т	Time
Lowerc	case subscripts (pp) and their meanings:		
рр			
2	to	mc	MCLR
ck	CLKOUT	osc	oscillator
су	cycle time	os	OSC1
drt	device reset timer	tO	TOCKI
io	I/O port	wdt	watchdog timer
Upperc	case letters and their meanings:		
S			
F	Fall	P	Period
н	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 16-1: LOAD CONDITIONS - PIC16C58A



16.7 Timing Diagrams and Specifications

FIGURE 16-2: EXTERNAL CLOCK TIMING - PIC16C58A

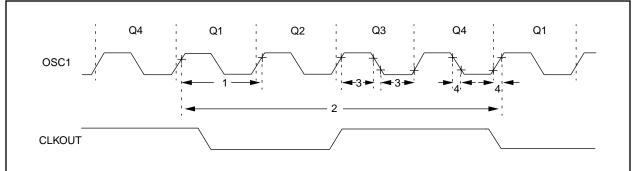


TABLE 16-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C58A

AC Characteristics									
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions		
	Fosc	External CLKIN Frequency ⁽²⁾	DC	-	4.0	MHz	XT osc mode		
			DC	_	2.0	MHz	XT osc mode (PIC16LV58A)		
			DC	—	4.0	MHz	HS osc mode (04)		
			DC	—	10	MHz	HS osc mode (10)		
			DC	—	20	MHz	HS osc mode (20)		
			DC	—	200	kHz	LP osc mode		
		Oscillator Frequency ⁽²⁾	DC		4.0	MHz	RC osc mode		
			DC	—	2.0	MHz	RC osc mode (PIC16LV58A)		
			0.1	—	4.0	MHz	XT osc mode		
			0.1	—	2.0	MHz	XT osc mode (PIC16LV58A)		
			4.0	—	4.0	MHz	HS osc mode (04)		
			4.0	—	10	MHz	HS osc mode (10)		
			4.0	—	20	MHz	HS osc mode (20)		
			5.0	—	200	kHz	LP osc mode		

These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (Tcy) equals four times the input oscillator time base period.

AC Chara	cteristics	$\begin{array}{lll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \ (commercial) \\ & -40^{\circ}C \leq TA \leq +85^{\circ}C \ (industrial) \\ & -20^{\circ}C \leq TA \leq +85^{\circ}C \ (industrial - PIC16LV58A) \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \ (extended) \\ \mbox{Operating Voltage VDD range is described in Section 16.1, Section 16.2 and Section 16.3.} \end{array}$									
Parameter No.	Sym	Characteristic Min Typ ⁽¹⁾ Max Units Conditions									
1	Tosc	External CLKIN Period ⁽²⁾	250	_	_	ns	XT osc mode				
			500	_	_	ns	XT osc mode (PIC16LV58A)				
			250	_	_	ns	HS osc mode (04)				
			100	_	_	ns	HS osc mode (10)				
			50	_	_	ns	HS osc mode (20)				
			5.0	_	_	μs	LP osc mode				
		Oscillator Period ⁽²⁾	250	_	—	ns	RC osc mode				
			500	_	_	ns	RC osc mode (PIC16LV58A)				
			250	_	10,000	ns	XT osc mode				
			500	_	_	ns	XT osc mode (PIC16LV58A)				
			250	_	250	ns	HS osc mode (04)				
			100	_	250	ns	HS osc mode (10)				
			50	_	250	ns	HS osc mode (20)				
			5.0	_	200	μs	LP osc mode				
2	Тсү	Instruction Cycle Time ⁽³⁾	—	4/Fosc	—	—					
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	_	_	ns	XT oscillator				
			20*	_	_	ns	HS oscillator				
			2.0*	_	_	μs	LP oscillator				
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	_		25*	ns	XT oscillator				
			_	_	25*	ns	HS oscillator				
			_	_	50*	ns	LP oscillator				

TABLE 16-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C58A (CON'T)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

vvnen an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all device

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 16-3: CLKOUT AND I/O TIMING - PIC16C58A

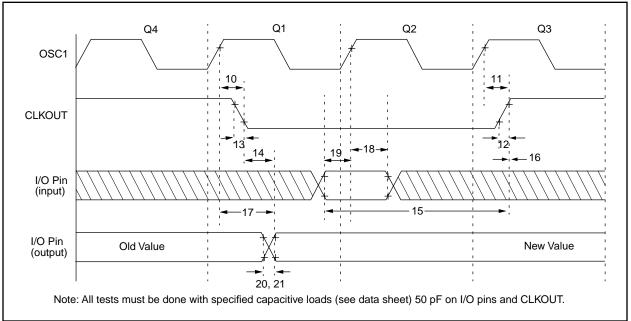


TABLE 16-3: CLKOUT AND I/O TIMING REQ	UIREMENTS - PIC16C58A
---------------------------------------	-----------------------

AC Chara	cteristics	$-40^{\circ}C \le TA \le -20^{\circ}C \le $	+70°C (comme +85°C (industri +85°C (industri +125°C (extend	rcial) al) al - PIC ded)	16LV58A)	5.2 and
Parameter No.	Sym	Characteristic	Min	Тур ⁽¹⁾	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽²⁾	_	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽²⁾	_	15	30**	ns
12	TckR	CLKOUT rise time ⁽²⁾	_	5	15**	ns
13	TckF	CLKOUT fall time ⁽²⁾	_	5	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽²⁾	_	_	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑ ⁽²⁾	0.25 TCY+30*	_		ns
16	TckH2iol	Port in hold after CLKOUT↑ ⁽²⁾	0*	_		ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid ⁽³⁾	—	_	100*	ns
18	TosH2iol	OSC1 [↑] (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	-	_	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	-		ns
20	TioR	Port output rise time ⁽³⁾	_	10	25**	ns
21	TioF	Port output fall time ⁽³⁾	_	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

3: See Figure 16-1 for loading conditions.

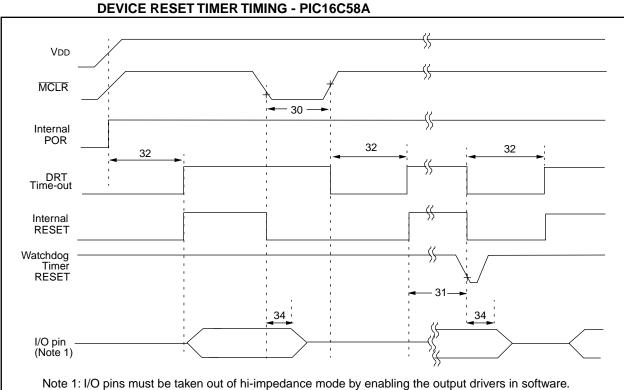


FIGURE 16-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C58

TABLE 16-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C58A

AC Characteristics		$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \ (commercial) \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \ (industrial) \\ -20^{\circ}C \leq TA \leq +85^{\circ}C \ (industrial - PIC16LV58A) \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \ (extended) \end{array}$									
		Operating Voltage VDD range is described in Section 16.1, Section 16.2 and Section 16.3.									
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions				
30	TmcL	MCLR Pulse Width (low)	100* 1μs	_	_	ns	VDD = 5.0V VDD = 5.0V (PIC16LV58A only)				
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)				
32	Tdrt	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)				
34	Tioz	I/O Hi-impedance from MCLR		_	100* 1μs	ns	(PIC16LV58A only)				

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 16-5: TIMER0 CLOCK TIMINGS - PIC16C58A

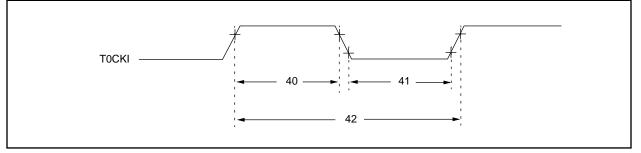


TABLE 16-5: TIMER0 CLOCK REQUIREMENTS - PIC16C58A

AC	Operating Ten	$\begin{array}{llllllllllllllllllllllllllllllllllll$							
Parameter No.	Sym	Characteristic		Min	Typ ⁽¹⁾	Мах	Units	Conditions	
40	Tt0H	T0CKI High Pulse Width - No Presc	aler	0.5 TCY + 20*	—	_	ns		
		- With Pres	scaler	10*	_		ns		
41	Tt0L	T0CKI Low Pulse Width - No Presc	aler	0.5 Tcy + 20*	—	—	ns		
		- With Pres	scaler	10*	_	_	ns		
42	Tt0P	T0CKI Period		20 or <u>Tcy + 40</u> * N			ns	Whichever is greater. N = Prescale Value (1, 2, 4,, 256)	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

NOTES:

17.0 ELECTRICAL CHARACTERISTICS - PIC16CR58A

Absolute Maximum Ratings†

5.	
Ambient Temperature under bias	–55°C to +125°C
Storage Temperature	65°C to +150°C
Voltage on VDD with respect to Vss	0 to +7.5V
Voltage on MCLR with respect to Vss	0 to +14V
Voltage on all other pins with respect to Vss	–0.6V to (VDD + 0.6V)
Total Power Dissipation ⁽¹⁾	800 mW
Max. Current out of Vss pin	150 mA
Max. Current into VDD pin	
Max. Current into an input pin (T0CKI only)	±500 μA
Input Clamp Current, Iк (VI < 0 or VI > VDD)	±20 mA
Output Clamp Current, IOK (VO < 0 or VO> VDD)	±20 mA
Max. Output Current sunk by any I/O pin	
Max. Output Current sourced by any I/O pin	20 mA
Max. Output Current sourced by a single I/O port (PORTA or B)	50 mA
Max. Output Current sunk by a single I/O port (PORTA or B)	50 mA
Note 1: Power Dissipation is calculated as follows: PDIS = VDD x {IDD - Σ IOH} + Σ {(VDD + Σ IOH) + Σ {(VD + Σ IOH) +	о-Voh) x Ioh} + Σ (Vol x Iol)

[†]NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 17-1:CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS
AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16CR58A-04	PIC16CR58A-10	PIC16CR58A-20	PIC16LCR58A-04
RC	VDD: 3.0V to 6.25V IDD: 2.5 mA max at 5.5V IPD: 4.0 μA max at 3.0V, WDT dis Freq: 4.0 MHz max	N/A	N/A	N/A
ХТ	VDD: 3.0V to 6.25V IDD: 2.5 mA max at 5.5V IPD: 4.0 μA max at 3.0V, WDT dis Freq: 4.0 MHz max	N/A	N/A	N/A
HS	N/A	VDD: 4.5V to 5.5V IDD: 8.0 mA max at 5.5V IPD: 4.0 μA max at 3.0V, WDT dis Freq: 10 MHz max	VDD: 4.5V to 5.5V IDD: 17 mA max at 5.5V IPD: 4.0 μA max at 3.0V, WDT dis Freq: 20 MHz max	N/A
LP	N/A	N/A	N/A	 VDD: 2.5V to 6.25V IDD: 28 μA max at 32 kHz, 2.5V IPD: 4.0 μA max at 2.5V, WDT dis Freq: 200 kHz max

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

17.1 DC Characteristics: PIC16CR58A-04, 10, 20 (Commercial) PIC16CR58A-04I, 10I, 20I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ (commercial) $-40^{\circ}C \le TA \le +85^{\circ}C$ (industrial)						
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions		
Supply Voltage RC and XT options HS option	Vdd	3.0 4.5		6.25 5.5	V V			
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP mode		
VDD Start Voltage to ensure Power-on Reset	VPOR		Vss		V	See Section 7.4 for details on Power-on Reset		
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset		
Supply Current ⁽³⁾ RC ⁽⁴⁾ and XT options HS option	IDD		1.9 2.5 4.7	2.5 8.0 17	mA mA mA	Fosc = 4.0 MHz, Vdd = 5.5V Fosc = 10 MHz, Vdd = 5.5V Fosc = 20 MHz, Vdd = 5.5V		
Power-Down Current ⁽⁵⁾ Commercial	IPD		4.0 0.25	12 4.0	μΑ μΑ	VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled		
Industrial			4.0 0.25	14 5.0	μΑ μΑ	VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled		

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

17.2 DC Characteristics: PIC16CR58A-04E, 10E, 20E (Extended)

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ (extended)							
Characteristic Sym			Typ ⁽¹⁾	Max	Units	Conditions		
Supply Voltage	Vdd							
RC and XT options		3.25		6.0	V			
HS options		4.5		5.5	V			
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP mode		
VDD Start Voltage to ensure Power-on Reset	VPOR		Vss		V	See Section 7.4 for details on Power-on Reset		
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset		
Supply Current ⁽³⁾	IDD							
RC ⁽⁴⁾ and XT options			1.9	3.3	mA	Fosc = 4.0 MHz, VDD = 5.5V		
HS option			4.8	10	mA	Fosc = 10 MHz, VDD = 5.5V		
			9.0	20	mA	Fosc = 20 MHz, VDD = 5.5V		
Power-Down Current ⁽⁵⁾	IPD							
			5.0	22	μA	VDD = 3.25V, WDT enabled		
			0.8	18	μA	VDD = 3.25V, WDT disabled		

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
- 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
- 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
- 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

17.3 DC Characteristics: PIC16LCR58A-04 (Commercial) PIC16LCR58A-04I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \le TA \le +70^{\circ}C$ (commercial) $-40^{\circ}C \le TA \le +85^{\circ}C$ (industrial)						
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions		
Supply Voltage	Vdd	2.5		6.25	V	LP option		
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP mode		
VDD Start Voltage to ensure Power-on Reset	VPOR		Vss		V	See Section 7.4 for details on Power-on Reset		
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset		
Supply Current ⁽³⁾ Commercial Industrial	IDD		12 15	28 37	μΑ μΑ	Fosc = 32 kHz, VDD = 2.5V, WDT disabled Fosc = 32 kHz, VDD = 2.5V, WDT disabled		
Power-Down Current⁽⁵⁾ Commercial Industrial	IPD		3.5 0.2 3.5 0.2	12 4.0 14 5.0	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled		

* These parameters are characterized but not tested.

- Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
 - 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to V_{ss} , T0CKI = VDD, $\overline{MCLR} = VDD$; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
 - 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
 - 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

17.4 DC Characteristics: PIC16CR58A-04, 10, 20, PIC16LCR58A-04 (Commercial) PIC16CR58A-04I, 10I, 20I, PIC16LCR58A-04I (Industrial)

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions (unless otherwise specified)Operating Temperature $0^{\circ}C \leq TA \leq +70^{\circ}C$ (commercial) $-40^{\circ}C \leq TA \leq +85^{\circ}C$ (industrial)Operating Voltage VDD range is described in Section 17.1 and Section 17.3.								
Characteristic	Sym	Min				Conditions				
			Ч¥Г	IVIAA	Units	Conditions				
Input Low Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	VIL	Vss Vss Vss Vss Vss		0.2 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V	Pin at hi-impedance RC option only ⁽⁴⁾ XT, HS and LP options				
Input High Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	Vih	0.45 VDD 2.0 0.36 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD		VDD VDD VDD VDD VDD VDD VDD	V V V V V V	For all VDD ⁽⁵⁾ $4.0V < VDD \le 5.5V^{(5)}$ VDD > 5.5V RC option only ⁽⁴⁾ XT, HS and LP options				
Hysteresis of Schmitt Trigger inputs	VHYS	0.15Vdd*			V					
Input Leakage Current ⁽³⁾ I/O ports MCLR T0CKI	IIL.	-1.0 -5.0 -3.0	0.5 0.5	+1.0 +5.0 +3.0	μΑ μΑ μΑ μΑ	For VDD \leq 5.5V VSS \leq VPIN \leq VDD, Pin at hi-impedance VPIN = VSS + 0.25V ⁽²⁾ VPIN = VDD ⁽²⁾ VSS \leq VPIN \leq VDD				
OSC1		-3.0	0.5	+3.0	μΑ	VSS \leq VPIN \leq VDD, XT, HS and LP options				
Output Low Voltage I/O ports OSC2/CLKOUT	Vol			0.6 0.6	V V	IOL = 8.7 mA, VDD = 4.5V IOL = 1.6 mA, VDD = 4.5V, RC option only				
Output High Voltage ⁽³⁾ I/O ports OSC2/CLKOUT	Vон	Vdd -0.7 Vdd -0.7			V V	IOH = -5.4 mA, VDD = 4.5V IOH = -1.0 mA, VDD = 4.5V, RC option only				

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

- 3: Negative current is defined as coming out of the pin.
- 4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.
- 5: The user may use the better of the two specifications.

17.5 DC Characteristics: PIC16CR58A-04E, 10E, 20E (Extended)

DC Characteristics All Pins Except Power Supply Pins		Operating Te	emperati	ire -	-40°C ≤ 1	otherwise specified) Γa ≤ +125°C (extended) n Section 17.2.
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions
Input Low Voltage I/O ports MCLR (Schmitt Trigger) TOCKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	VIL	Vss Vss Vss Vss Vss		0.2 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V	Pin at hi-impedance RC option only ⁽⁴⁾ XT, HS and LP options
Input High Voltage I/O ports MCLR (Schmitt Trigger) TOCKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	Vih	0.45 VDD 2.0 0.36 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD		VDD VDD VDD VDD VDD VDD VDD	> > > > > > > > >	For all VDD ⁽⁵⁾ $4.0V < VDD \le 5.5V^{(5)}$ VDD > 5.5V RC option only ⁽⁴⁾ XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	VHYS	0.15Vdd*			V	
Input Leakage Current ⁽³⁾ I/O ports MCLR T0CKI OSC1	IIL.	-1.0 -5.0 -3.0 -3.0	0.5 0.5 0.5	+1.0 +5.0 +3.0 +3.0	μΑ μΑ μΑ μΑ μΑ	For VDD \leq 5.5V VSS \leq VPIN \leq VDD, Pin at hi-impedance VPIN = VSS + 0.25V ⁽²⁾ VPIN = VDD ⁽²⁾ VSS \leq VPIN \leq VDD VSS \leq VPIN \leq VDD XT, HS and LP options
Output Low Voltage I/O ports OSC2/CLKOUT	Vol			0.6 0.6	V V	IOL = 8.7 mA, VDD = 4.5V IOL = 1.6 mA, VDD = 4.5V, RC option only
Output High Voltage⁽³⁾ I/O ports OSC2/CLKOUT	Vон	Vdd0.7 Vdd0.7			V V	IOH = -5.4 mA, VDD = 4.5V IOH = -1.0 mA, VDD = 4.5V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

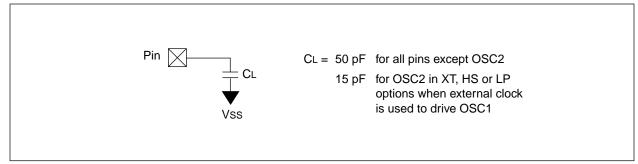
17.6 <u>Timing Parameter Symbology and Load Conditions</u>

The timing parameter symbols have been created following one of the following formats:

- 1. TppS2ppS
- 2. TppS

2. Tpp3			
т			
F	Frequency	Т	Time
Lowerc	ase subscripts (pp) and their meanings:		
рр			
2	to	mc	MCLR
ck	CLKOUT	osc	oscillator
су	cycle time	os	OSC1
drt	device reset timer	tO	TOCKI
io	I/O port	wdt	watchdog timer
Upperc	case letters and their meanings:		
S			
F	Fall	P	Period
н	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 17-1: LOAD CONDITIONS - PIC16CR58A



17.7 **Timing Diagrams and Specifications**

FIGURE 17-2: EXTERNAL CLOCK TIMING - PIC16CR58A

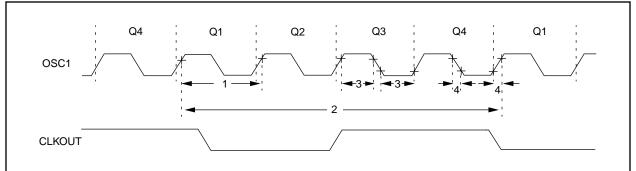


TABLE 17-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR58A

AC Characteristics		$ \begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \ (commercial) \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \ (industrial) \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \ (extended) \\ \mbox{Operating Voltage VDD range is described in Section 17.1, Section 17.2 and Section 17.3.} \end{array} $							
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions		
	Fosc	External CLKIN Frequency ⁽²⁾	DC	—	4.0	MHz	XT osc mode		
			DC	—	4.0	MHz	HS osc mode (04)		
			DC	—	10	MHz	HS osc mode (10)		
			DC	—	20	MHz	HS osc mode (20)		
			DC	—	200	kHz	LP osc mode		
		Oscillator Frequency ⁽²⁾	DC	-	4.0	MHz	RC osc mode		
			0.1	—	4.0	MHz	XT osc mode		
			4.0	—	4.0	MHz	HS osc mode (04)		
			4.0	—	10	MHz	HS osc mode (10)		
			4.0	—	20	MHz	HS osc mode (20)		
			5.0	—	200	kHz	LP osc mode		
* These pa	rameters are	characterized but not tested	4.0		20	MHz	HS osc mode (20)		

These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (Tcy) equals four times the input oscillator time base period.

TABLE 17-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR58A (CON'T)

AC Characteristics		$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \ (commercial) \\ & -40^{\circ}C \leq TA \leq +85^{\circ}C \ (industrial) \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \ (extended) \\ \mbox{Operating Voltage VDD range is described in Section 17.1, Section 17.2 and Section 17.3.} \end{array}$							
Parameter No.	Sym	Characteristic Min Typ ⁽¹⁾ Max Units Conditions							
1	Tosc	External CLKIN Period ⁽²⁾	250	_	_	ns	XT osc mode		
			250	_	_	ns	HS osc mode (04)		
			100	_	_	ns	HS osc mode (10)		
			50	_	_	ns	HS osc mode (20)		
			5.0	_	_	μs	LP osc mode		
		Oscillator Period ⁽²⁾	250	_	—	ns	RC osc mode		
			250	—	10,000	ns	XT osc mode		
			250	—	250	ns	HS osc mode (04)		
			100	—	250	ns	HS osc mode (10)		
			50	—	250	ns	HS osc mode (20)		
			5.0	—	200	μs	LP osc mode		
2	Тсү	Instruction Cycle Time ⁽³⁾	_	4/Fosc	—				
3	TosL, TosH	Clock in (OSC1) Low or High Time	85*	_	_	ns	XT oscillator		
			20*	_	_	ns	HS oscillator		
			2.0*	_	_	μs	LP oscillator		
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	_	_	25*	ns	XT oscillator		
			_	_	25*	ns	HS oscillator		
			—	_	50*	ns	LP oscillator		

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 17-3: CLKOUT AND I/O TIMING - PIC16CR58A

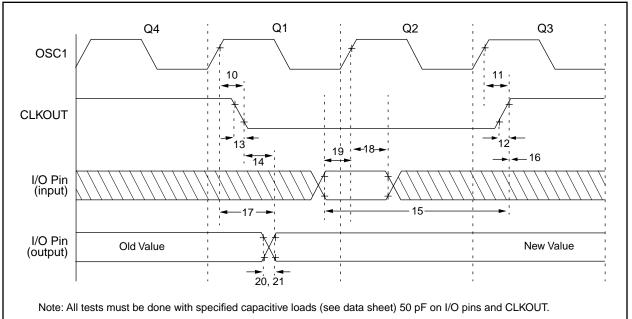


TABLE 17-3-	CLKOUT AND I/O TIMING REQUIREMENTS - PIC16CR58A
TADLL TT-J.	CERCUT AND I/O TIMING REQUIREMENTS - FICTOCISOA

AC Chara	cteristics	-40°C ≤ TA ≤	+70°C (comme +85°C (industri +125°C (extend	rcial) al) ded)		7.2 and
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽²⁾	_	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽²⁾		15	30**	ns
12	TckR	CLKOUT rise time ⁽²⁾		5.0	15**	ns
13	TckF	CLKOUT fall time ⁽²⁾		5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽²⁾	_	_	40**	ns
15	TioV2ckH	Port in valid before CLKOUT ⁽²⁾	0.25 TCY+30*	_	_	ns
16	TckH2iol	Port in hold after CLKOUT ⁽²⁾	0*	_	_	ns
17	TosH2ioV	OSC1 [↑] (Q1 cycle) to Port out valid ⁽³⁾	_	_	100*	ns
18	TosH2iol	OSC1 [↑] (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1 [↑] (I/O in setup time)	TBD	-	—	ns
20	TioR	Port output rise time ⁽³⁾	—	10	25**	ns
21	TioF	Port output fall time ⁽³⁾	_	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

3: See Figure 17-1 for loading conditions.

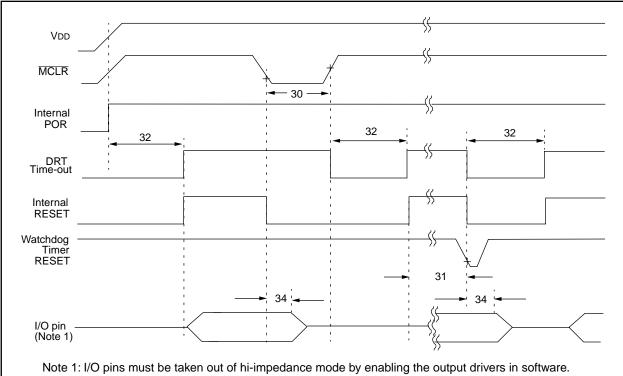


FIGURE 17-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16CR58A

TABLE 17-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16CR58A

AC Charac	teristics	$ \begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ (commercial)} \\ & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ (industrial)} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ (extended)} \\ \mbox{Operating Voltage VDD range is described in Section 17.1, Section 17.2 and Section 17.3.} \end{array} $						
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions	
30	TmcL	MCLR Pulse Width (low)	1.0*	—	_	μs	VDD = 5.0V	
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)	
32	Tdrt	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)	
34	Tioz	I/O Hi-impedance from MCLR Low		_	1.0*	μs		

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 17-5: TIMER0 CLOCK TIMINGS - PIC16CR58A

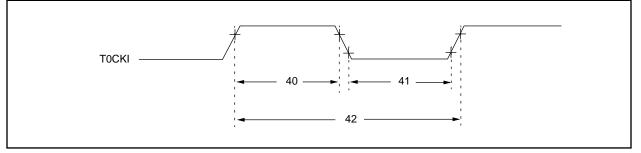


TABLE 17-5: TIMER0 CLOCK REQUIREMENTS - PIC16CR58A

AC Characteristics			$\begin{array}{llllllllllllllllllllllllllllllllllll$							
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Мах	Units	Conditions			
40	Tt0H	T0CKI High Pulse V	Vidth - No Prescaler	0.5 TCY + 20*	—	_	ns			
			- With Prescaler	10*	_	_	ns			
41	Tt0L	T0CKI Low Pulse W	Vidth - No Prescaler	0.5 TCY + 20*	—	-	ns			
			- With Prescaler	10*	—	-	ns			
42	Tt0P	T0CKI Period		20 or <u>Tcy + 40</u> * N		_	ns	Whichever is greater. N = Prescale Value (1, 2, 4,, 256)		

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

NOTES:

18.0 DC AND AC CHARACTERISTICS - PIC16C54A/CR57B/C58A/CR58A

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean - 3σ) respectively, where σ is standard deviation.

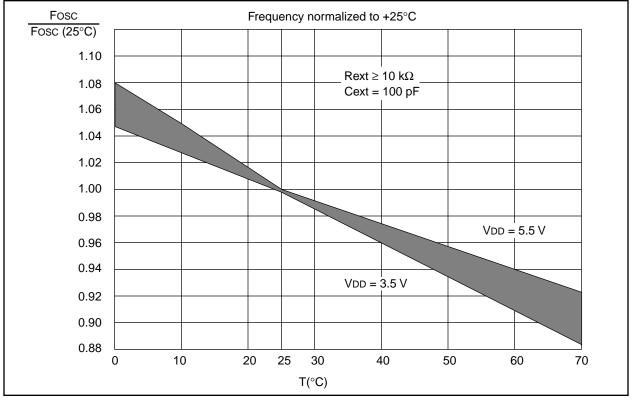


FIGURE 18-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

 TABLE 18-1:
 RC OSCILLATOR FREQUENCIES

Cext	Rext		rage 5 V, 25°C
20 pF	3.3 k	4.973 MHz	± 27%
	5 k	3.82 MHz	± 21%
	10 k	2.22 MHz	± 21%
	100 k	262.15 kHz	± 31%
100 pF	3.3 k	1.63 MHz	± 13%
	5 k	1.19 MHz	± 13%
	10 k	684.64 kHz	± 18%
	100 k	71.56 kHz	± 25%
300 pF	3.3 k	660 kHz	± 10%
	5.0 k	484.1 kHz	± 14%
	10 k	267.63 kHz	± 15%
	160 k	29.44 kHz	± 19%

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ± 3 standard deviation from average value for VDD = 5 V.

FIGURE 18-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20 PF

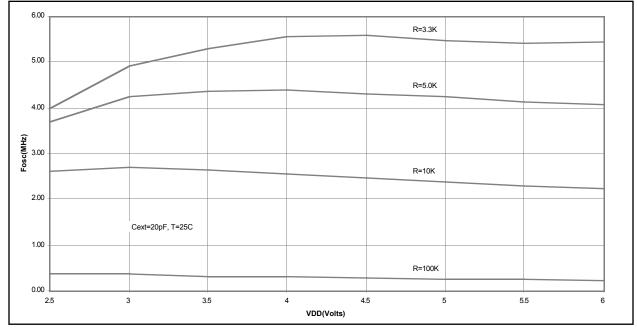
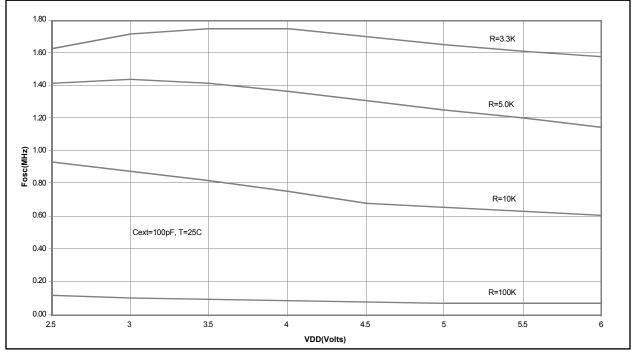


FIGURE 18-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 100 PF



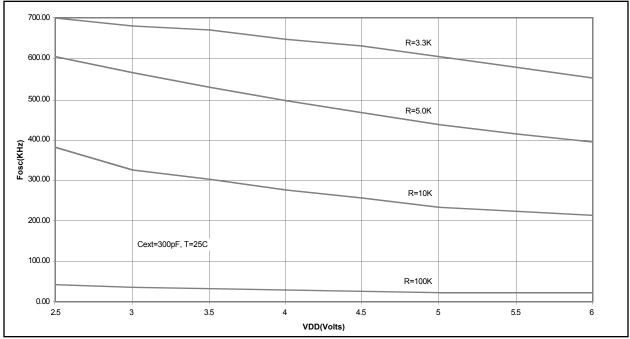
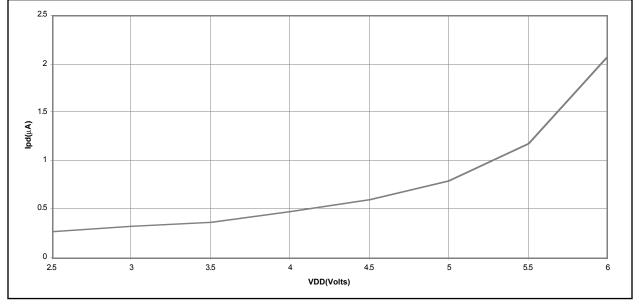


FIGURE 18-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 PF





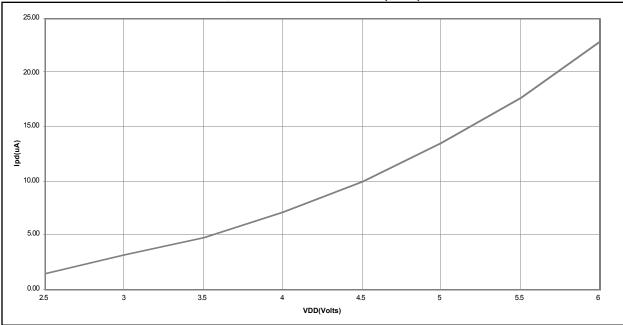
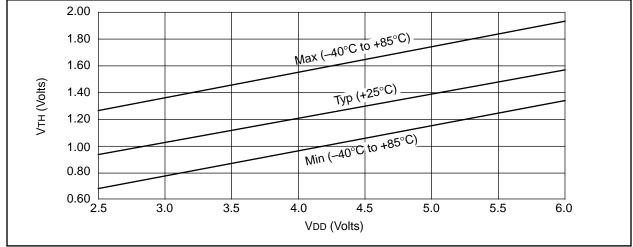


FIGURE 18-6: TYPICAL IPD vs. VDD, WATCHDOG ENABLED (25°C)





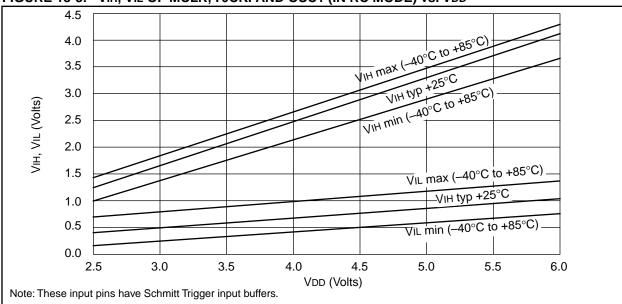


FIGURE 18-8: VIH, VIL OF MCLR, TOCKI AND OSC1 (IN RC MODE) vs. VDD



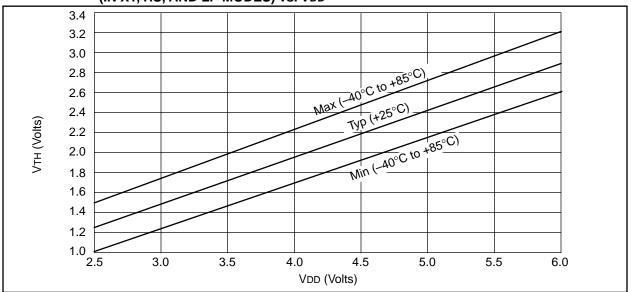


FIGURE 18-10: TYPICAL IDD vs. FREQUENCY (WDT DIS, RC MODE @ 20 PF, 25°C)

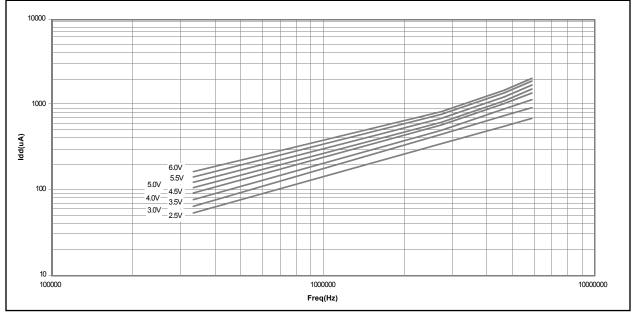
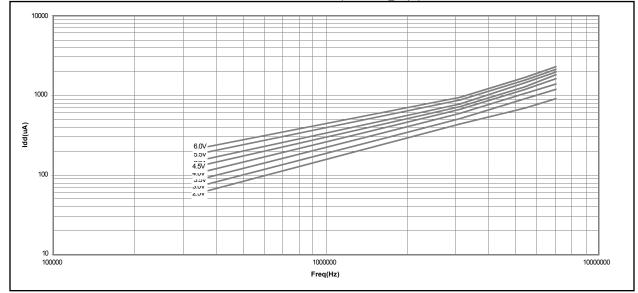


FIGURE 18-11: MAXIMUM IDD vs. FREQUENCY (WDT DIS, RC MODE @ 20 PF, -40°C TO +85°C)



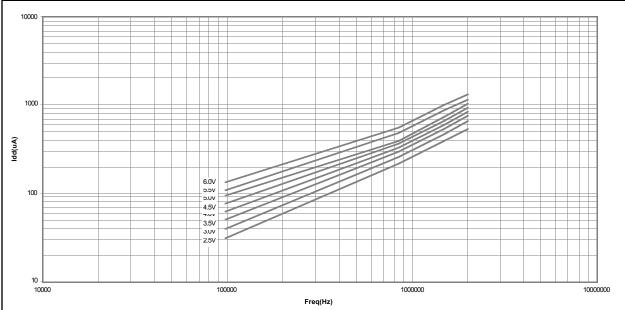


FIGURE 18-12: TYPICAL IDD vs. FREQUENCY (WDT DIS, RC MODE @ 100 PF, 25°C)



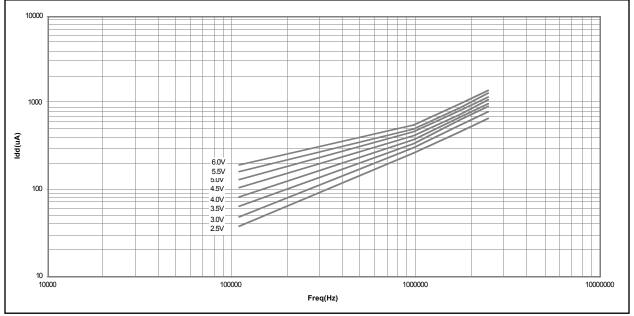


FIGURE 18-14: TYPICAL IDD vs. FREQUENCY (WDT DIS, RC MODE @ 300 PF, 25°C)

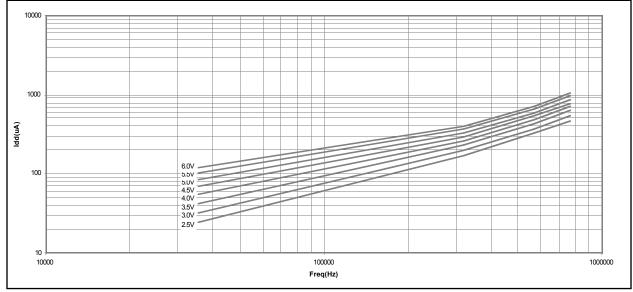
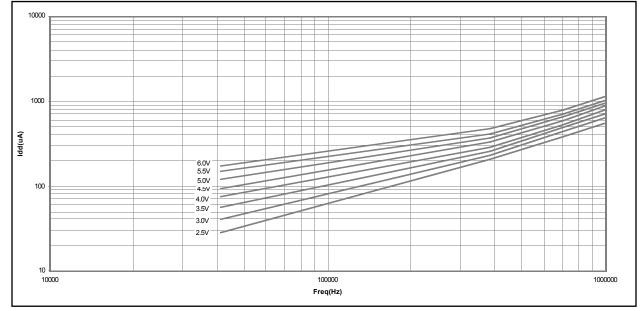


FIGURE 18-15: MAXIMUM IDD vs. FREQUENCY (WDT DIS, RC MODE @ 300 PF, -40°C TO +85°C)



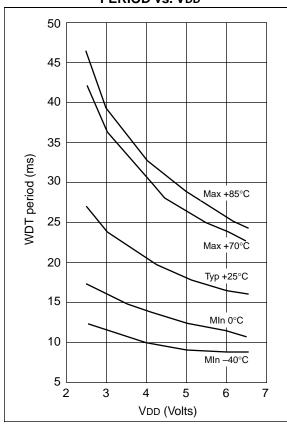


FIGURE 18-16: WDT TIMER TIME-OUT PERIOD vs. VDD

TABLE 18-2:INPUT CAPACITANCE FOR
PIC16C54A/C58A

Pin	Typical Capacitance (pF)					
FIII	18L PDIP	18L SOIC				
RA port	5.0	4.3				
RB port	5.0	4.3				
MCLR	17.0	17.0				
OSC1	4.0	3.5				
OSC2/CLKOUT	4.3	3.5				
тоскі	3.2	2.8				

All capacitance values are typical at 25° C. A part-to-part variation of $\pm 25\%$ (three standard deviations) should be taken into account.

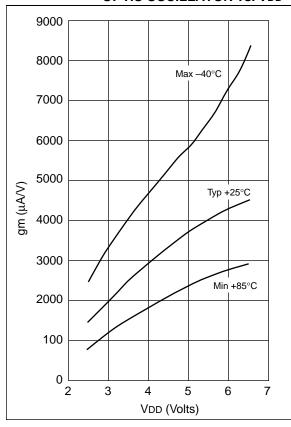


FIGURE 18-17: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD

FIGURE 18-18: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD

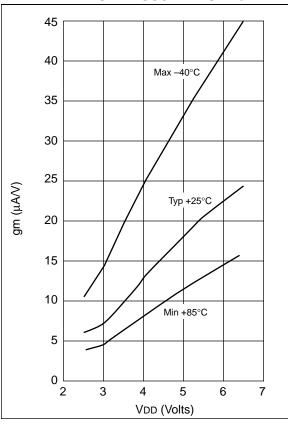


FIGURE 18-19: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD

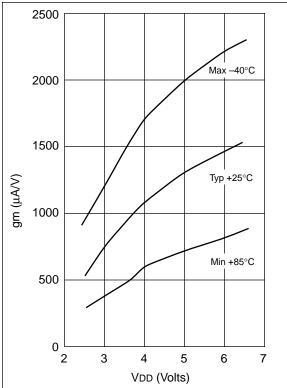


FIGURE 18-20: IOH vs. VOH, VDD = 3 V

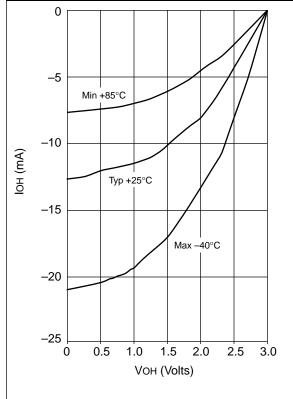


FIGURE 18-21: IOH vs. VOH, VDD = 5 V

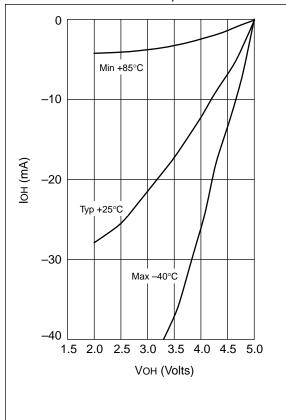


FIGURE 18-22: IOL vs. VOL, VDD = 3 V

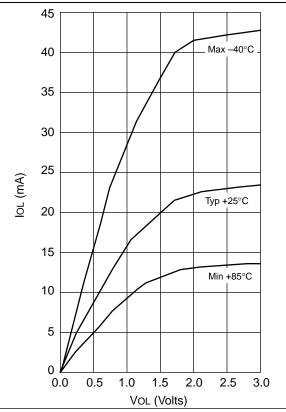
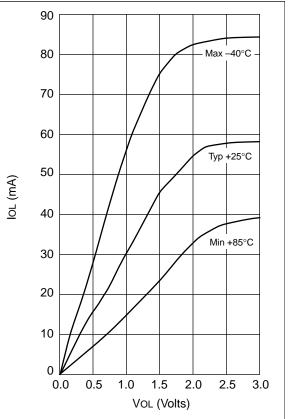


FIGURE 18-23: IOL vs. VOL, VDD = 5 V



NOTES:

19.0 ELECTRICAL CHARACTERISTICS -PIC16C54B/CR54B/C56A/CR56A/C58B/CR58B

Absolute Maximum Ratings[†]

Ambient temperature under bias	–55°C to +125°C
Storage temperature	
Voltage on VDD with respect to Vss	
Voltage on MCLR with respect to Vss	
Voltage on all other pins with respect to Vss	
Total power dissipation ⁽¹⁾	
Max. current out of Vss pin	
Max. current into VDD pin	
Max. current into an input pin (T0CKI only)	
Input clamp current, IK (VI < 0 or VI > VDD)	
Output clamp current, IOK (VO < 0 or VO > VDD)	
Max. output current sunk by any I/O pin	
Max. output current sourced by any I/O pin	
Max. output current sourced by a single I/O port A	
Max. output current sourced by a single I/O port B	
Max. output current sunk by a single I/O port A	
Max. output current sunk by a single I/O port B	
Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - \sum IOH} + \sum {(VDD-V	
[†] NOTICE: Stresses above those listed under "Maximum Ratings" may cause permaner This is a stress rating only and functional operation of the device at those or any other indicated in the operation listings of this specification is not implied. Exposure to maxim extended periods may affect device reliability.	conditions above those

TABLE 19-1:CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS
AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C5X-04	PIC16C5X-20	PIC16C5X/JW
RC	VDD: 3.0V to 5.5V IDD: 2.4 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 4 MHz max.	VDD: 3.0V to 5.5V IDD: 1.7 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 5.5V IDD: 2.4 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 4.0 MHz max.
хт	VDD: 3.0V to 5.5V IDD 2.4 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 4 MHz max.	VDD: 3.0V to 5.5V IDD: 1.7 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 5.5V IDD 2.4 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 4.0 MHz max.
нѕ	N/A	VDD: 4.5V to 5.5V IDD: 16 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 20 MHz max.	 VDD: 4.5V to 5.5V IDD: 16 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 20 MHz max.
LP	VDD: 3.0V to 5.5V IDD: 14 μA typ. at 32kHz, 3.0V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 200 kHz max.	Do not use in LP mode	VDD: 3.0V to 5.5V IDD: 32 μA max. at 32kHz, 3.0V WDT dis IPD: 4.0 μA max. at 3.0V WDT dis Freq: 200 kHz max.

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

19.1 DC Characteristics: PIC16C5X-04, 20 (Commercial) PIC16CR5X-04, 20 (Commercial) PIC16CR5X-04I, 20 (Commercial) PIC16C5X-04I, 20I (Industrial) PIC16CR5X-04I, 20I (Industrial)

DC Characteristics Power Supply Pins		$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ (commercial)} \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ (industrial)} \end{array}$						
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions		
Supply Voltage XT, RC and LP options HS option	Vdd	3.0 4.5		5.5 5.5	V V			
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP mode		
VDD start voltage to ensure Power-On Reset	VPOR		Vss		V	See Section 7.4 for details on Power-on Reset		
VDD rise rate to ensure Power-On Reset	Svdd	0.05*			V/ms	See Section 7.4 for details on Power-on Reset		
Supply Current ⁽³⁾ XT and RC ⁽⁴⁾ options HS option LP option, Commercial LP option, Industrial	IDD		1.8 4.5 14 17	2.4 16 32 40	mA	Fosc = 4.0 MHz, VDD = $5.5V$ Fosc = 20 MHz, VDD = $5.5V$ Fosc = 32 kHz, VDD = $3.0V$, WDT disabled Fosc = 32 kHz, VDD = $3.0V$, WDT disabled		
Power Down Current⁽⁵⁾ Commercial Industrial	IPD		4.0 0.25 4.0 0.25	12 4.0 14 5.0	μΑ μΑ μΑ μΑ	VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled VDD = 3.0V, WDT enabled VDD = 3.0V, WDT disabled		

* These parameters are characterized but not tested.

- Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
 - 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, \overline{MCLR} = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
 - 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
 - 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

19.2 DC Characteristics: PIC16C5X-04E, 20E (Extended) PIC16CR5X-04E, 20E (Extended)

DC Characteristics Power Supply Pins			Standard Operating Conditions (unless otherwise specified)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$ (extended)						
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions			
Supply Voltage	Vdd								
XT and RC options		3.0		5.5	V V				
HS option		4.5		5.5	V				
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP mode			
VDD start voltage to ensure Power-On Reset	VPOR		Vss		V	See Section 7.4 for details on Power-on Reset			
VDD rise rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset			
Supply Current ⁽³⁾	IDD								
XT and RC ⁽⁴⁾ options			1.8	3.3	mA	Fosc = 4.0 MHz, VDD = 5.5V			
HS option			9.0	20	mA	FOSC = 20 MHz, VDD = 5.5 V			
Power Down Current ⁽⁵⁾	IPD		0.3	18	μA	VDD = 3.5V, WDT disabled			
			4.5	22	μA	VDD = 3.5V, WDT enabled			

* These parameters are characterized but not tested.

- Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
 - 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
 - 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled toVss, TOCKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
 - 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
 - 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

19.3 <u>DC Characteristics:</u> <u>PIC16LCR5X-04 (Commercial)</u> <u>PIC16LCR5X-04I (Industrial)</u>

DC Characteristics Power Supply Pins					re	tions (unless otherwise specified) $0^{\circ}C \le TA \le +70^{\circ}C$ (commercial) $40^{\circ}C \le TA \le +85^{\circ}C$ (industrial)
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions
Supply Voltage XT and RC options LP options	Vdd	3.0 2.5		5.5 5.5	V V	
RAM Data Retention Voltage ⁽²⁾	Vdr		1.5*		V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR		Vss		V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See Section 7.4 for details on Power-on Reset
Supply Current ⁽³⁾ XT and RC ⁽⁴⁾ options LP option, Commercial LP option, Industrial	IDD		0.5 11 14	2.4 27 35		Fosc = 4.0 MHz, VDD = $5.5V$ Fosc = 32 kHz, VDD = $2.5V$ WDT disabled Fosc = 32 kHz, VDD = $2.5V$ WDT disabled
Power Down Current⁽⁵⁾ Commercial Industrial	IPD		2.5 0.25 2.5 0.25	12 4.0 14 5.0	μΑ μΑ μΑ μΑ	VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled VDD = 2.5V, WDT enabled VDD = 2.5V, WDT enabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

- 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
- 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
- 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and Vss.

19.4 DC Characteristics: PIC16C5X-04, 20, PIC16LCR5X-04 (Commercial) PIC16CR5X-04, 20, PIC16CR5X-04I, 20I (Commercial) PIC16C5X-04I, 20I, PIC16LC5X-04I (Industrial) PIC16C5X-04E, 20E (Extended)

DC Characteristics All Pins Except Power Supply Pins		$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions		
Input Low Voltage I/O Ports I/O Ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	VIL	Vss Vss Vss Vss Vss		0.8 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.15 VDD 0.3 VDD	V V V V	Pin at hi-impedance 4.5V , VDD \leq 5.5V Pin at hi-impedance 2.5V , VDD \leq 4.5V RC option only ⁽⁴⁾ XT, HS and LP options		
Input High Voltage I/O ports MCLR (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	Vih	0.25 VDD+0.8V 2.0 0.85 VDD 0.85 VDD 0.85 VDD 0.85 VDD 0.7 VDD		Vdd Vdd Vdd Vdd Vdd Vdd	V V V V V	For all V _{DD} (5) 4.5V < V _{DD} ≤ 5.5V ⁽⁵⁾ RC option only ⁽⁴⁾ XT, HS and LP options		
Hysteresis of Schmitt Trigger inputs	VHYS	0.15Vdd*			V			
Input Leakage Current ⁽³⁾ I/O ports MCLR T0CKI OSC1	lı.	-1.0 -5.0 -3.0 -3.0	0.5 0.5 0.5 0.5	+1.0 +5.0 +3.0 +3.0	μΑ μΑ μΑ μΑ μΑ	For VDD \leq 5.5V Vss \leq VPIN \leq VDD, Pin at hi-impedance VPIN = Vss +0.25V ⁽²⁾ VPIN = VDD ⁽²⁾ Vss \leq VPIN \leq VDD Vss \leq VPIN \leq VDD,		
Output Low Voltage I/O ports OSC2/CLKOUT	Vol			0.6 0.6	V V	XT, HS and LP options IOL = 8.7 mA, VDD = 4.5V IOL = 1.6 mA, VDD = 4.5V, RC option only		
Output High Voltage I/O ports ⁽³⁾ OSC2/CLKOUT	Vон	Vdd-0.7 Vdd-0.7			V V	IOH = -5.4 mA, VDD = 4.5V IOH = -1.0 mA, VDD = 4.5V, RC option only		

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

19.5 <u>Timing Parameter Symbology and Load Conditions</u>

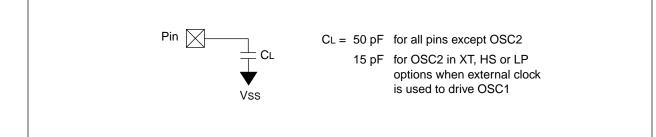
The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS

2. TppS			-	-	
	2.1	「ppS			

_2. Tpp5			
Т			
F	Frequency	Т	Time
Lowerc	ase subscripts (pp) and their meanings:		
рр			
2	to	mc	MCLR
ck	CLKOUT	osc	oscillator
су	cycle time	os	OSC1
drt	device reset timer	tO	TOCKI
io	I/O port	wdt	watchdog timer
Upperc	ase letters and their meanings:		
S			
F	Fall	P	Period
н	High	R	Rise
1	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 19-1: LOAD CONDITIONS - PIC16C54B/CR54B/C56A/CR56A/C58B/CR58B, PIC16CR5X



19.6 <u>Timing Diagrams and Specifications</u>

FIGURE 19-2: EXTERNAL CLOCK TIMING - PIC16C5X, PIC16CR5X

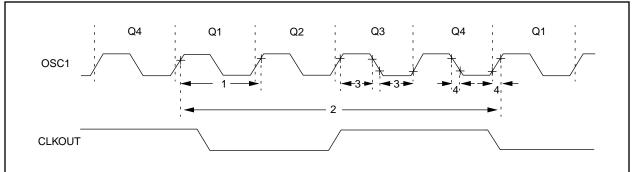


TABLE 19-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Characteristics		$\begin{array}{lll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \ (commercial) \\ -40^{\circ}C \leq TA \leq +85^{\circ}C \ (industrial) \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \ (extended) \\ \mbox{Operating Voltage VDD range is described in Section 19.1, Section 19.2 and Section 19.3.} \end{array}$								
Parameter No.	Sym	Characteristic	Min	Тур ⁽¹⁾	Max	Units	Conditions			
	Fosc	External CLKIN Frequency ⁽²⁾	DC	_	4.0	MHz	XT osc mode			
			DC	_	4.0	MHz	HS osc mode (04)			
			DC	_	20	MHz	HS osc mode (20)			
			DC	_	200	kHz	LP osc mode			
		Oscillator Frequency ⁽²⁾	DC	_	4.0	MHz	RC osc mode			
			0.455	—	4.0	MHz	XT osc mode			
			4	—	4.0	MHz	HS osc mode (04)			
			4	—	20	MHz	HS osc mode (20)			
			5	—	200	kHz	LP osc mode			
1	Tosc	External CLKIN Period ⁽²⁾	250	_	_	ns	XT osc mode			
			250	—	—	ns	HS osc mode (04)			
			50	—	—	ns	HS osc mode (20)			
			5.0	—	—	μs	LP osc mode			
		Oscillator Period ⁽²⁾	250	_	_	ns	RC osc mode			
			250	-	2,200	ns	XT osc mode			
			250	-	250	ns	HS osc mode (04)			
			50	-	250	ns	HS osc mode (20)			
			5.0	_	200	μs	LP osc mode			

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (Tcy) equals four times the input oscillator time base period.

TABLE 19-2: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X (CON'T)

AC Characteristics		$\begin{array}{ll} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ (commercial)} \\ & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ (industrial)} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ (extended)} \\ \mbox{Operating Voltage VDD range is described in Section 19.1, Section 19.2 and Section 19.3.} \end{array}$							
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions		
2	Тсү	Instruction Cycle Time ⁽³⁾	_	4/Fosc	_	_			
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*			ns	XT oscillator		
			20*	—	—	ns	HS oscillator		
			2.0*	—		μs	LP oscillator		
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—		25*	ns	XT oscillator		
			_	—	25*	ns	HS oscillator		
			_	—	50*	ns	LP oscillator		

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

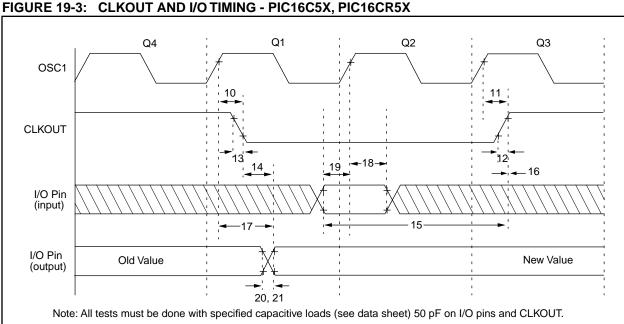


TABLE 19-3: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Char	acteristics	$\begin{array}{llllllllllllllllllllllllllllllllllll$							
Parameter No.	Sym	Characteristic	Min	Тур ⁽¹⁾	Мах	Units			
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽²⁾	_	15	30**	ns			
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽²⁾	_	15	30**	ns			
12	TckR	CLKOUT rise time ⁽²⁾		5.0	15**	ns			
13	TckF	CLKOUT fall time ⁽²⁾	_	5.0	15**	ns			
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽²⁾	_	_	40**	ns			
15	TioV2ckH	Port in valid before CLKOUT ⁽²⁾	0.25 TCY+30*	_	_	ns			
16	TckH2iol	Port in hold after CLKOUT↑ ⁽²⁾	0*	_	_	ns			
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid ⁽³⁾	_	_	100*	ns			
18	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	_	ns			
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	_	ns			
20	TioR	Port output rise time ⁽³⁾	_	10	25**	ns			
21	TioF	Port output fall time ⁽³⁾	_	10	25**	ns			

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

3: See Figure 19-1 for loading conditions.

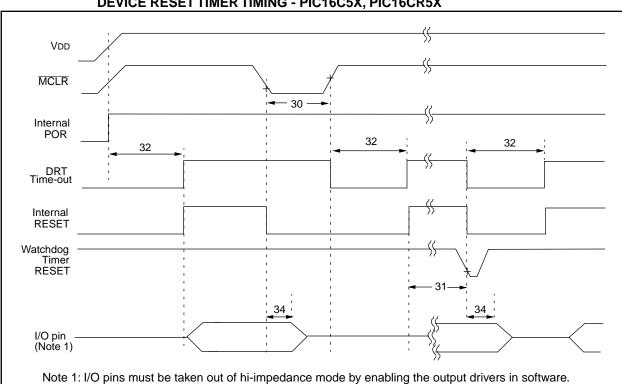


FIGURE 19-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X, PIC16CR5X

TABLE 19-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X, PIC16CR5X

AC Charac	teristics	$ \begin{array}{l} \mbox{Standard Operating Conditions (unless otherwise specified)} \\ \mbox{Operating Temperature} & 0^{\circ}C \leq TA \leq +70^{\circ}C \mbox{ (commercial)} \\ & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ (industrial)} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ (extended)} \\ \mbox{Operating Voltage VDD range is described in Section 19.1, Section 19.2 and Section 19.3.} \end{array} $					
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	1000*	_	—	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)
32	Tdrt	Device Reset Timer Period		18*	30*	ms	VDD = 5.0V (Commercial)
34	Tioz	I/O Hi-impedance from MCLR Low	100*	300*	1000*	ns	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 19-5: TIMER0 CLOCK TIMINGS - PIC16C5X, PIC16CR5X

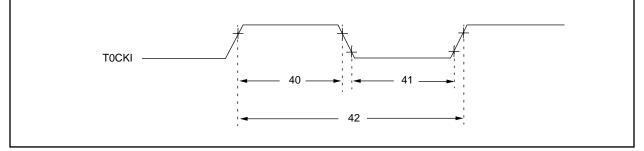


TABLE 19-5: TIMER0 CLOCK REQUIREMENTS - PIC16C5X, PIC16CR5X

AC	Chara	Operating Tempera	$\begin{array}{llllllllllllllllllllllllllllllllllll$				
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Мах	Units	Conditions
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	_	_	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	_	ns	
		- With Prescaler	10*	—	_	ns	
42	Tt0P	T0CKI Period	20 or <u>Tcy + 40</u> * N	_	_	ns	Whichever is greater. N = Prescale Value (1, 2, 4,, 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

20.0 DC AND AC CHARACTERISTICS -PIC16C54B/CR54B/C56A/CF56A/C58B/CR58B

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean - 3σ) respectively, where σ is standard deviation.

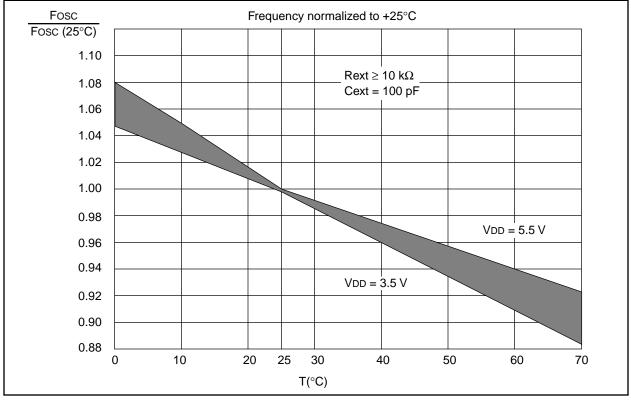


FIGURE 20-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

TABLE 20-1: RC	OSCILLATOR FREQU	ENCIES
----------------	-------------------------	--------

Cext	Rext		rage 5V, 25°C
20 pF	3.3 k	4.973 MHz	± 27%
	5 k	3.82 MHz	± 21%
	10 k	2.22 MHz	± 21%
	100 k	262.15 kHz	± 31%
100 pF	3.3 k	1.63 MHz	± 13%
	5 k	1.19 MHz	± 13%
	10 k	684.64 kHz	± 18%
	100 k	71.56 kHz	± 25%
300 pF	3.3 k	660 kHz	± 10%
	5.0 k	484.1 kHz	± 14%
	10 k	267.63 kHz	± 15%
	160 k	29.44 kHz	± 19%

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ± 3 standard deviation from average value for VDD = 5 V.

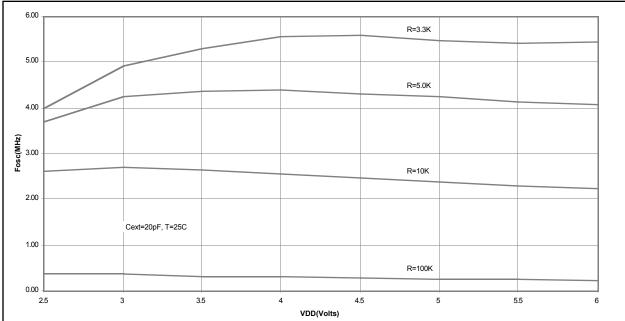
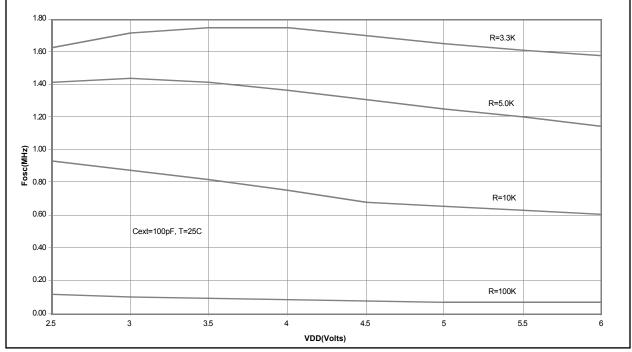


FIGURE 20-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20 PF





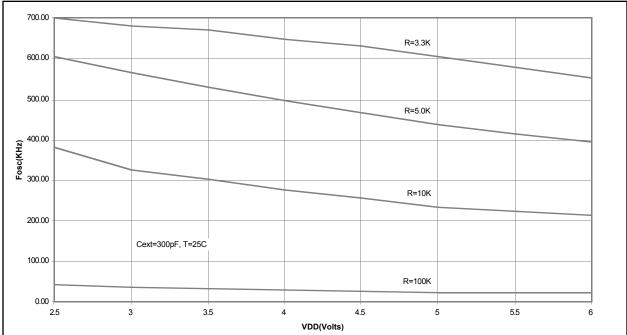
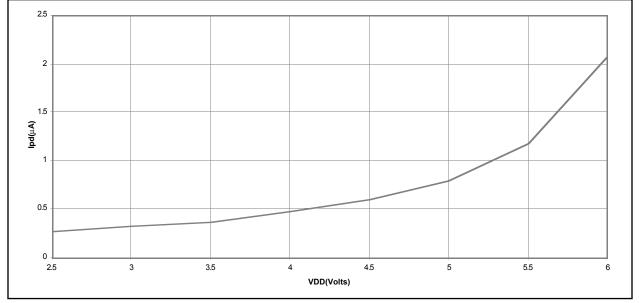
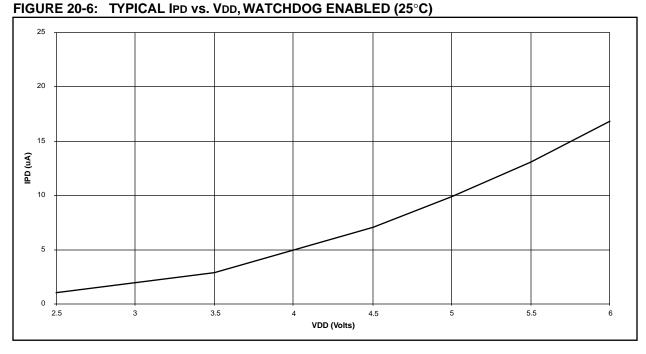
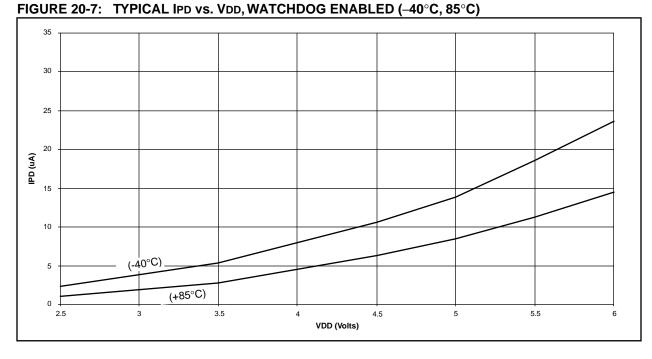


FIGURE 20-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 PF









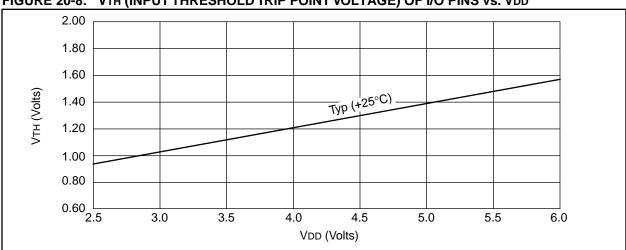


FIGURE 20-8: VTH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF I/O PINS vs. VDD



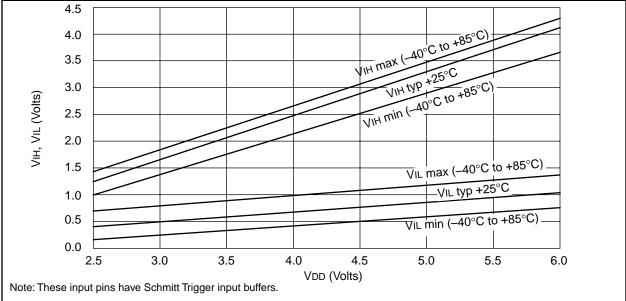


FIGURE 20-10: VTH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs. Vdd

PIC16C5X

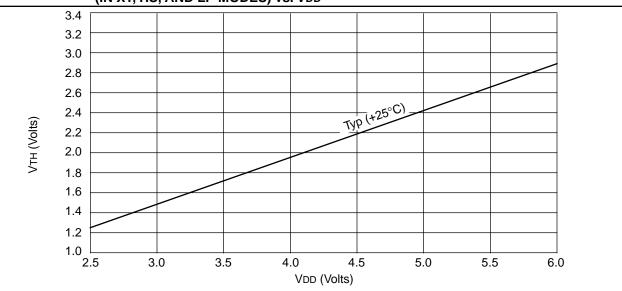
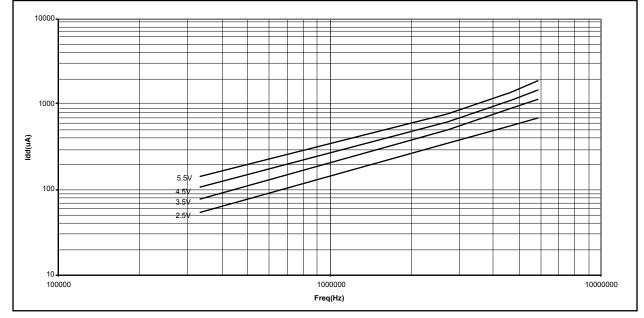


FIGURE 20-11: TYPICAL IDD vs. FREQUENCY (WDT DIS, RC MODE @ 20 PF, 25°C)



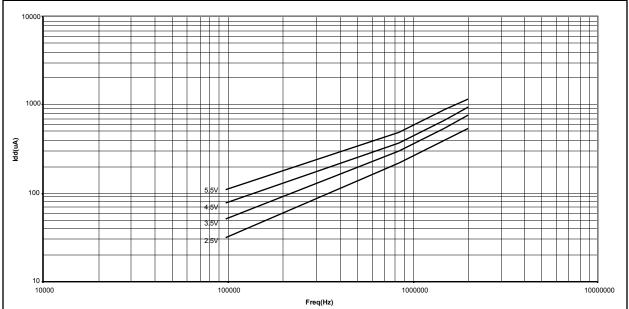


FIGURE 20-12: TYPICAL IDD vs. FREQUENCY (WDT DIS, RC MODE @ 100 PF, 25°C)



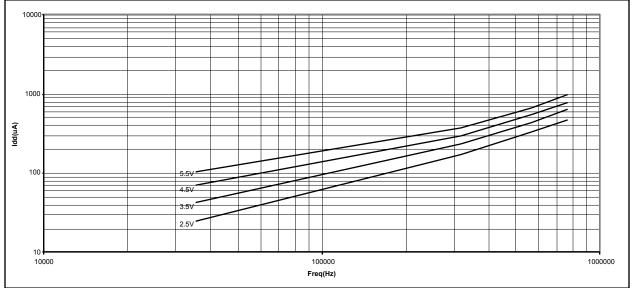


FIGURE 20-14: WDT TIMER TIME-OUT PERIOD vs. VDD

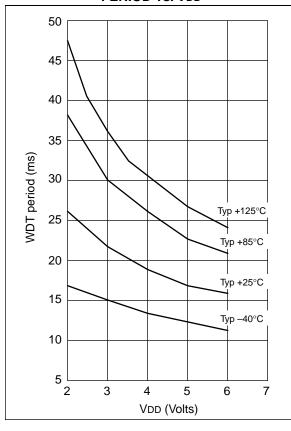


TABLE 20-2:INPUT CAPACITANCE FOR
PIC16C54s/C58s

Pin	Typical Capacitance (pF)			
FIII	18L PDIP	18L SOIC		
RA port	5.0	4.3		
RB port	5.0	4.3		
MCLR	17.0	17.0		
OSC1	4.0	3.5		
OSC2/CLKOUT	4.3	3.5		
TOCKI	3.2	2.8		

All capacitance values are typical at 25°C. A part-to-part variation of \pm 25% (three standard deviations) should be taken into account.

FIGURE 20-15: IOH vs. VOH, VDD = 3 V

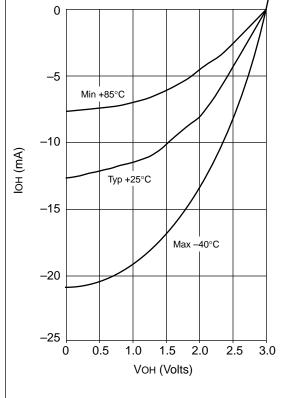


FIGURE 20-16: IOH vs. VOH, VDD = 5 V

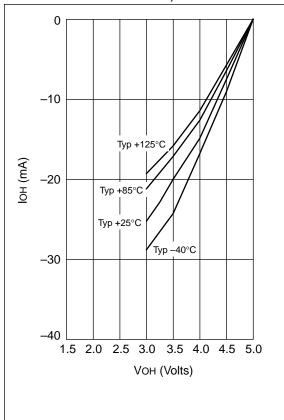


FIGURE 20-17: IOL vs. VOL, VDD = 3 V

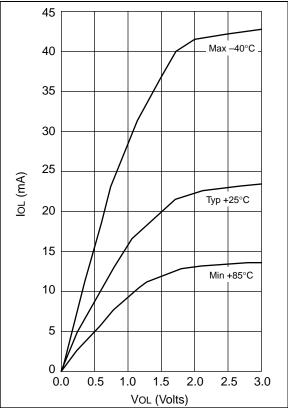
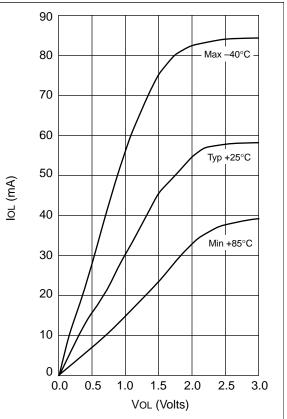


FIGURE 20-18: IOL vs. VOL, VDD = 5 V



21.0 PACKAGING INFORMATION

21.1 Package Marking Information

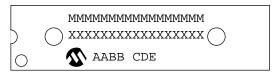
18-Lead PDIP



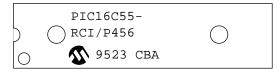
Example



28-Lead Skinny PDIP (.300")

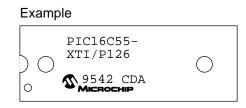


Example



28-Lead PDIP (.600")





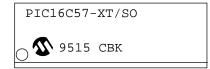
Legend	d: MMM	Microchip part number information
	XXX	Customer specific information*
	AA	Year code (last two digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	С	Facility code of the plant at which wafer is manufactured
		C = Chandler, Arizona, U.S.A.,
		S = Tempe, Arizona, U.S.A.
	D	Mask revision number
	Е	Assembly code of the plant or country of origin in which
		part was assembled
Note:	In the ever	nt the full Microchip part number cannot be marked on one line,
	it will be c	arried over to the next line thus limiting the number of available
	characters	s for customer specific information.
* Sta	andard OTF	P marking consists of Microchip part number, year code, week
COC	de, facility	code, mask rev#, and assembly code. For OTP marking
bey	ond this, c	ertain price adders apply. Please check with your Microchip
Sa	les Office.	For QTP devices, any special marking adders are included in
QT	P price.	



28-Lead SOIC



Example



20-Lead SSOP



28-Lead SSOP

 MMMMMMMM XXXXXXXX
CDE

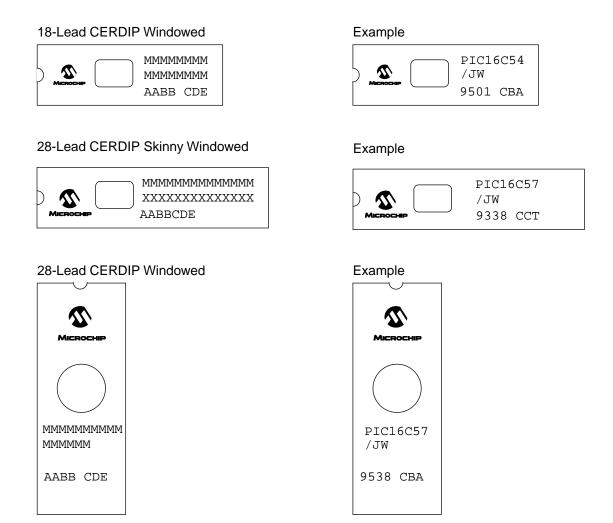
Example



Example

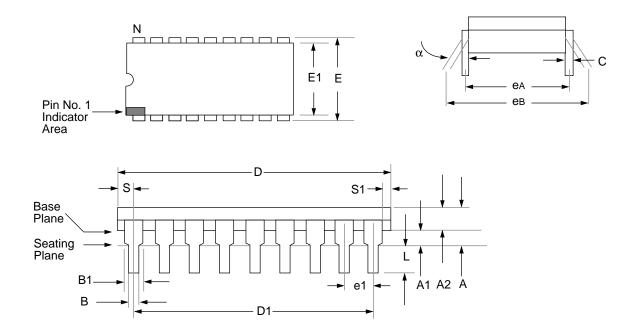


Legend: MMN	Microchip part number information
XX>	Customer specific information*
AA	Year code (last two digits of calendar year)
BB	Week code (week of January 1 is week '01')
C	Facility code of the plant at which wafer is manufactured
	C = Chandler, Arizona, U.S.A.,
	S = Tempe, Arizona, U.S.A.
D	Mask revision number
E	Assembly code of the plant or country of origin in which
	part was assembled
Note: In the ev	vent the full Microchip part number cannot be marked on one line,
	carried over to the next line thus limiting the number of available
characte	ers for customer specific information.
code, facility	TP marking consists of Microchip part number, year code, week y code, mask rev#, and assembly code. For OTP marking , certain price adders apply. Please check with your Microchip e. For QTP devices, any special marking adders are included in



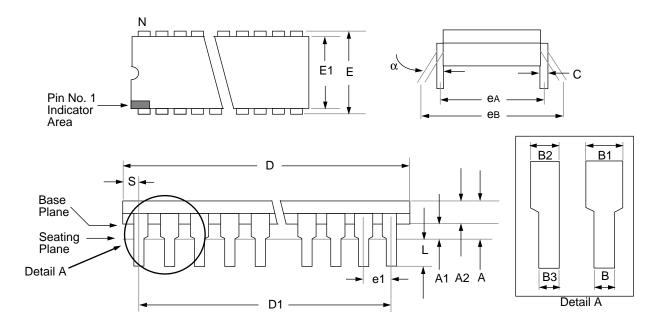
Legend	d: MMM	Microchip part number information
	XXX	Customer specific information*
	AA	Year code (last two digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	С	Facility code of the plant at which wafer is manufactured
		C = Chandler, Arizona, U.S.A.,
		S = Tempe, Arizona, U.S.A.
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which
		part was assembled
Note:	In the ever	nt the full Microchip part number cannot be marked on one line,
	it will be ca	arried over to the next line thus limiting the number of available
	characters	s for customer specific information.
		P marking consists of Microchip part number, year code, week
		code, mask rev#, and assembly code. For OTP marking
		ertain price adders apply. Please check with your Microchip
-		For QTP devices, any special marking adders are included in
QI	P price.	

21.2 <u>18-Lead Plastic Dual In-Line (PDIP) - 300 mil</u>



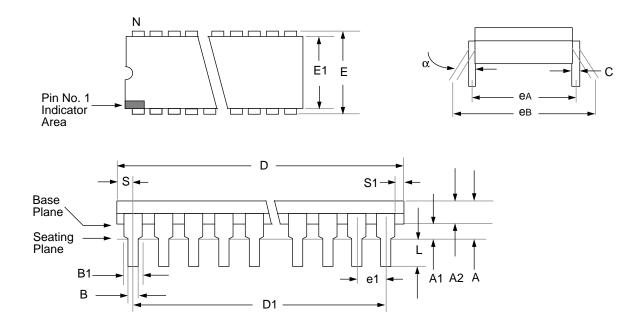
	Package Group: Plastic Dual In-Line (PLA)								
		Millimeters		Inches					
Symbol	Min	Мах	Notes	Min	Max	Notes			
α	0°	10°		0 °	10°				
А	_	4.064		_	0.160				
A1	0.381	-		0.015	_				
A2	3.048	3.810		0.120	0.150				
В	0.355	0.559		0.014	0.022				
B1	1.524	1.524	Reference	0.060	0.060	Reference			
С	0.203	0.381	Typical	0.008	0.015	Typical			
D	22.479	23.495		0.885	0.925				
D1	20.320	20.320	Reference	0.800	0.800	Reference			
E	7.620	8.255		0.300	0.325				
E1	6.096	7.112		0.240	0.280				
e1	2.489	2.591	Typical	0.098	0.102	Typical			
eA	7.620	7.620	Reference	0.300	0.300	Reference			
eB	7.874	9.906		0.310	0.390				
L	3.048	3.556		0.120	0.140				
N	18	18		18	18				
S	0.889	-		0.035	-				
S1	0.127	-		0.005	-				

21.3 <u>28-Lead Plastic Dual In-Line (PDIP) - 300 mil</u>



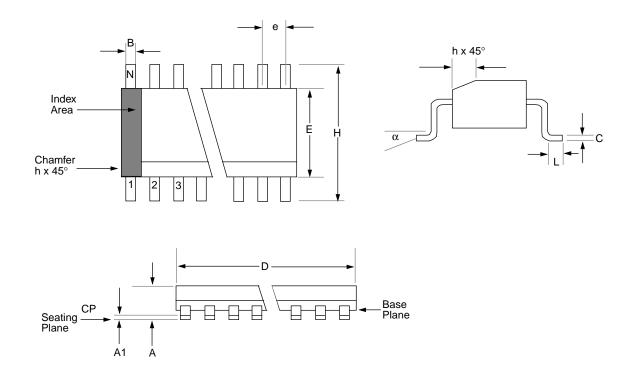
Package Group: Plastic Dual In-Line (PLA)							
		Millimeters		Inches			
Symbol	Min	Max	Notes	Min	Max	Notes	
α	0°	10°		0°	10°		
А	3.632	4.572		0.143	0.180		
A1	0.381	-		0.015	_		
A2	3.175	3.556		0.125	0.140		
В	0.406	0.559		0.016	0.022		
B1	1.016	1.651	Typical	0.040	0.065	Typical	
B2	0.762	1.016	4 places	0.030	0.040	4 places	
B3	0.203	0.508	4 places	0.008	0.020	4 places	
С	0.203	0.331	Typical	0.008	0.013	Typical	
D	34.163	35.179		1.385	1.395		
D1	33.020	33.020	Reference	1.300	1.300	Reference	
E	7.874	8.382		0.310	0.330		
E1	7.112	7.493		0.280	0.295		
e1	2.540	2.540	Typical	0.100	0.100	Typical	
eA	7.874	7.874	Reference	0.310	0.310	Reference	
eB	8.128	9.652		0.320	0.380		
L	3.175	3.683		0.125	0.145		
Ν	28	-		28	-		
S	0.584	1.220		0.023	0.048		

21.4 28-Lead Plastic Dual In-Line (PDIP) - 600 mil



	Package Group: Plastic Dual In-Line (PLA)							
		Millimeters		Inches				
Symbol	Min	Max	Notes	Min	Max	Notes		
α	0°	10°		0°	10°			
А	_	5.080		_	0.200			
A1	0.508	_		0.020	_			
A2	3.175	4.064		0.125	0.160			
В	0.355	0.559		0.014	0.022			
B1	1.270	1.778	Typical	0.050	0.070	Typical		
С	0.203	0.381	Typical	0.008	0.015	Typical		
D	35.052	37.084		1.380	1.460			
D1	33.020	33.020	Reference	1.300	1.300	Reference		
E	15.240	15.875		0.600	0.625			
E1	12.827	13.970		0.505	0.550			
e1	2.489	2.591	Typical	0.098	0.102	Typical		
eA	15.240	15.240	Reference	0.600	0.600	Reference		
eB	15.240	17.272		0.600	0.680			
L	2.921	3.683		0.115	0.145			
Ν	28	28		28	28			
S	0.889	-		0.035	_			
S1	0.508	_		0.020	-			

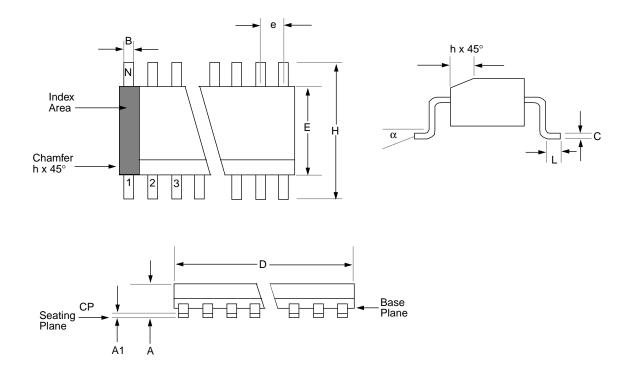
21.5 <u>18-Lead Plastic Surface Mount (SOIC) - 300 mil</u>



	Package Group: Plastic SOIC (SO)						
		Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Мах	Notes	
α	0°	8°		0°	8°		
А	2.362	2.642		0.093	0.104		
A1	0.101	0.300		0.004	0.012		
В	0.355	0.483		0.014	0.019		
С	0.241	0.318		0.009	0.013		
D	11.353	11.735		0.447	0.462		
Е	7.416	7.595		0.292	0.299		
е	1.270	1.270	Reference	0.050	0.050	Reference	
Н	10.007	10.643		0.394	0.419		
h	0.381	0.762		0.015	0.030		
L	0.406	1.143		0.016	0.045		
Ν	18	18		18	18		
CP	_	0.102		_	0.004		

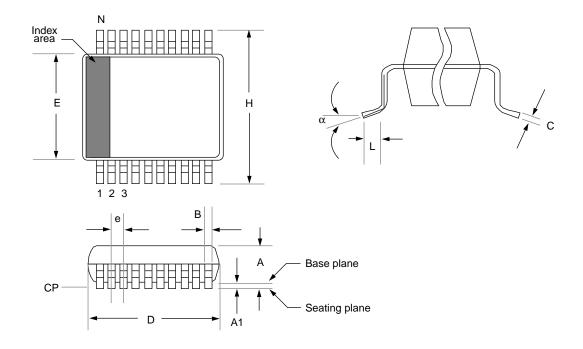
© 1997 Microchip Technology Inc.

21.6 <u>28-Lead Plastic Surface Mount (SOIC) - 300 mil</u>



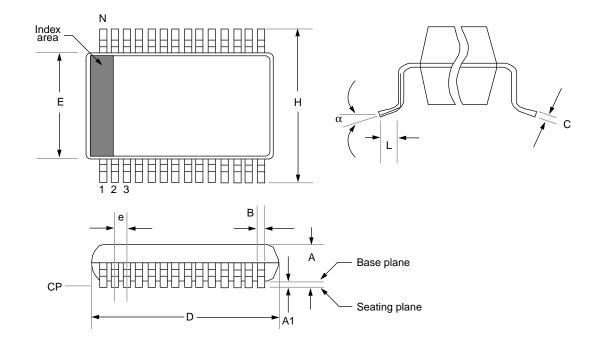
Package Group: Plastic SOIC (SO)							
		Millimeters		Inches			
Symbol	Min	Max	Notes	Min	Мах	Notes	
α	0°	8 °		0°	8 °		
А	2.362	2.642		0.093	0.104		
A1	0.101	0.300		0.004	0.012		
В	0.355	0.483		0.014	0.019		
С	0.241	0.318		0.009	0.013		
D	17.703	18.085		0.697	0.712		
E	7.416	7.595		0.292	0.299		
е	1.270	1.270	Typical	0.050	0.050	Typical	
Н	10.007	10.643		0.394	0.419		
h	0.381	0.762		0.015	0.030		
L	0.406	1.143		0.016	0.045		
Ν	28	28		28	28		
CP	-	0.102		-	0.004		

21.7 20-Lead Plastic Surface Mount (SSOP) - 209 mil



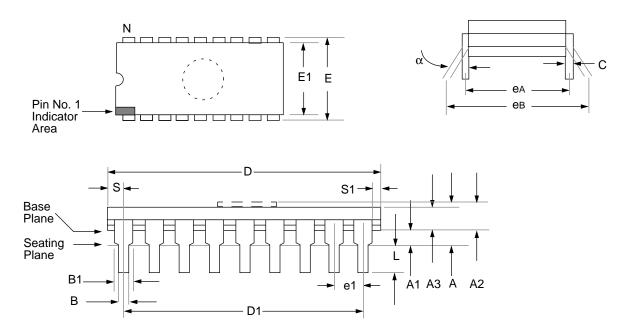
Package Group: Plastic SSOP							
		Millimeters		Inches			
Symbol	Min	Max	Notes	Min	Мах	Notes	
α	0°	8°		0°	8 °		
А	1.730	1.990		0.068	0.078		
A1	0.050	0.210		0.002	0.008		
В	0.250	0.380		0.010	0.015		
С	0.130	0.220		0.005	0.009		
D	7.070	7.330		0.278	0.289		
E	5.200	5.380		0.205	0.212		
е	0.650	0.650	Reference	0.026	0.026	Reference	
Н	7.650	7.900		0.301	0.311		
L	0.550	0.950		0.022	0.037		
N	20	20		20	20		
CP	-	0.102		-	0.004		

21.8 28-Lead Plastic Surface Mount (SSOP) - 209 mil



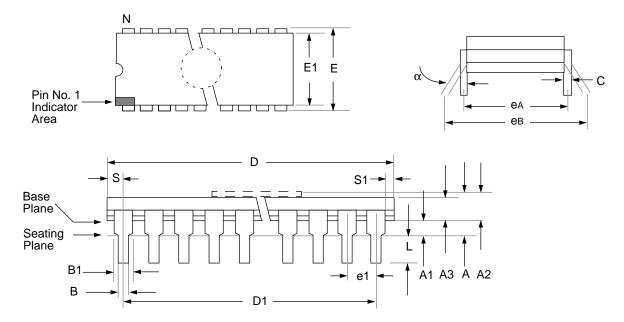
	Package Group: Plastic SSOP							
		Millimeters		Inches				
Symbol	Min	Мах	Notes	Min	Max	Notes		
α	0°	8 °		0°	8°			
А	1.730	1.990		0.068	0.078			
A1	0.050	0.210		0.002	0.008			
В	0.250	0.380		0.010	0.015			
С	0.130	0.220		0.005	0.009			
D	10.070	10.330		0.396	0.407			
E	5.200	5.380		0.205	0.212			
е	0.650	0.650	Reference	0.026	0.026	Reference		
Н	7.650	7.900		0.301	0.311			
L	0.550	0.950		0.022	0.037			
Ν	28	28		28	28			
CP	-	0.102		-	0.004			

21.9 <u>18-Lead Ceramic Dual In-Line (CERDIP) with Window - 300 mil</u>



		Package Gro	up: Ceramic Dual	In-Line (CDP)			
		Millimeters			Inches		
Symbol	Min	Max	Notes	Min	Max	Notes	
α	0°	10°		0°	10°		
А	_	5.080			0.200		
A1	0.381	1.7780		0.015	0.070		
A2	3.810	4.699		0.150	0.185		
A3	3.810	4.445		0.150	0.175		
В	0.355	0.585		0.014	0.023		
B1	1.270	1.651	Typical	0.050	0.065	Typical	
С	0.203	0.381	Typical	0.008	0.015	Typical	
D	22.352	23.622		0.880	0.930		
D1	20.320	20.320	Reference	0.800	0.800	Reference	
E	7.620	8.382		0.300	0.330		
E1	5.588	7.874		0.220	0.310		
e1	2.540	2.540	Reference	0.100	0.100	Reference	
eA	7.366	8.128	Typical	0.290	0.320	Typical	
eB	7.620	10.160		0.300	0.400		
L	3.175	3.810		0.125	0.150		
Ν	18	18		18	18		
S	0.508	1.397		0.020	0.055		
S1	0.381	1.270		0.015	0.050		

21.10 28-Lead Ceramic Dual In-Line (CERDIP) with Window - 600 mil



Package Group: Ceramic Dual In-Line (CDP)							
	Millimeters						
Symbol	Min	Max	Notes	Min	Мах	Notes	
α	0°	10°		0°	10°		
А	_	5.461			0.215		
A1	0.381	1.524		0.015	0.060		
A2	3.810	4.699		0.150	0.185		
A3	3.810	4.445		0.150	0.175		
В	0.355	0.585		0.014	0.023		
B1	1.270	1.651	Typical	0.050	0.065	Typical	
С	0.203	0.381	Typical	0.008	0.015	Typical	
D	36.195	37.465		1.425	1.475		
D1	33.020	33.020	Reference	1.300	1.300	Reference	
E	15.240	15.875		0.600	0.625		
E1	12.954	15.240		0.510	0.600		
e1	2.540	2.540	Typical	0.100	0.100	Typical	
eA	14.986	15.748	Reference	0.590	0.620	Reference	
eB	15.240	18.034		0.600	0.710		
L	3.175	3.810		0.125	0.150		
Ν	28	28		28	28		
S	1.016	2.286		0.040	0.090		
S1	0.381	1.778		0.015	0.070		

APPENDIX A: COMPATIBILITY

To convert code written for PIC16CXX to PIC16C5X, the user should take the following steps:

- 1. Check any CALL, GOTO or instructions that modify the PC to determine if any program memory page select operations (PA2, PA1, PA0 bits) need to be made.
- 2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
- 3. Eliminate any special function register page switching. Redefine data variables to reallocate them.
- 4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
- 5. Change reset vector to proper value for processor used.
- 6. Remove any use of the ADDLW and SUBLW instructions.
- 7. Rewrite any code segments that use interrupts.

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PART NO.	-XX Frequency Range	X │ Temperature Range	/XX Package	XXX Pattern		Exa a)	temp., PD	4A -04/P 301 = Commercial DIP package, 4MHz, normal VDD
Device	PIC16LC PIC16CF PIC16LC	5X ⁽²⁾ , PIC16C5X 5X ⁽²⁾ , PIC16LC 85X ⁽²⁾ , PIC16CR 85X ⁽²⁾ , PIC16L0 5X ⁽²⁾ , PIC16LV 5X ⁽²⁾ , PIC16LV5	5XT ⁽³⁾ 5XT ⁽³⁾ CR5XT ⁽³⁾			b) c)	PIC16LC SOIC pa limits. PIC16CR	TP pattern #301. 58A - 04I/SO = Industrial temp., ackage, 4MHz, Extended VDD R54A - 10I/P355 = ROM program Industrial temp., PDIP package,
Frequency Range	04 10 20	= 2 MHz = 4 MHz = 10 MHz = 20 MHz = No type for JV	V ⁽⁴⁾ devices			Note	1: b = 2: C	= Standard VDD range
Temperature Range	I	$= 0^{\circ}C \text{ to } +7$ = -40°C to +8 = -40°C to +12	5°C (Indus	strial)			CR	 = Extended VDD range = ROM Version, Standard VDD range R = ROM Version, Extended VDD
Package	P SO	= Windowed CE = PDIP = SOIC (Gull Wi = Skinny PDIP (= SSOP (209 m	ng, 300 mil l 28-pin, 300				3: T = 4: UV	range = Low Voltage VDD range in tape and reel - SOIC, SSOP packages only. erasable devices are tested to all ilable voltage/frequency options.
Pattern	3-digit Pa	attern Code for G	QTP, ROM (b	lank otherwis	se)		Eras 04. osci	The user can select 04, 10 or 20 illators by programmng the appro- te configuration bits.

PIC16C54/55/56/57 PRODUCT IDENTIFICATION SYSTEM

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PART NO. Device	-XX Oscillator	X Temperature	/XX Package	XXX Pattern	Exam	nples:
Device Oscillator Type	PIC16C PIC16C PIC16C RC LP XT HS	Range 554, PIC16C54T 55, PIC16C55T 56, PIC16C56T 57, PIC16C57T = Resistor Capa = Low Power Ci = Standard Crys = High Speed Ci	(2) (2) (2) vystal stal/Resonato crystal	pr	b) i c) d)	PIC16C54 - XT/PXXX = "XT" oscillator, commercial temp., PDIP, QTP pattern. PIC16C55 - XTI/SO = "XT" oscillator, industrial temp., SOIC (OTP device) PIC16C55 /JW = Commercial temp. CERDIP with window. PIC16C57 - RC/S = "RC" oscillator, com- mercial temp., dice in waffle pack.
Temperature Range	10 b ⁽¹⁾ l E	= 10 MHz Cryst = No type for JV = 0°C to +7 = -40°C to +8 = -40°C to +12	V ⁽³⁾ devices 0°C (Comme 5°C (Industria	al)	Note	 b = blank T = in tape and reel - SOIC, SSOP packages only. UV erasable devices are tested to all
Package	JW P SO SP SS	= Windowed CE = PDIP = Die in Waffle I = SOIC (Gull W = Skinny PDIP = SSOP (209 m	Pack ing, 300 mil b (28 pin, 300 n	• /		3. Overasable devices are tested to an available voltage/frequency options. Erased devices are oscillator type RC. The user can select RC, LP, XT or HS oscillators by programming the appropriate configuration bits.
Pattern	3-digit F	Pattern Code for	QTP (blank o	therwise)		

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Italy

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JAPAN

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