RS8973

Single-Chip SDSL/HDSL Transceiver

The RS8973 is a full-duplex 2B1Q transceiver based on Conexant's HDSL technology, with a built-in frequency synthesizer to support variable rate SDSL applications. It offers 2320 kbps operation, low power consumption, and pin-for-pin compatibility with Bt8970 and Bt8960.

The RS8973 is a highly integrated device that includes all of the active circuitry needed for a complete 2B1Q transceiver. In the receive portion of the device, a variable gain amplifier optimizes the signal level according to the dynamic range of the analog-to-digital converter. Once the signal is digitized, sophisticated adaptive echo cancellation, equalization, and detection DSP algorithms reproduce the originally transmitted far-end signal.

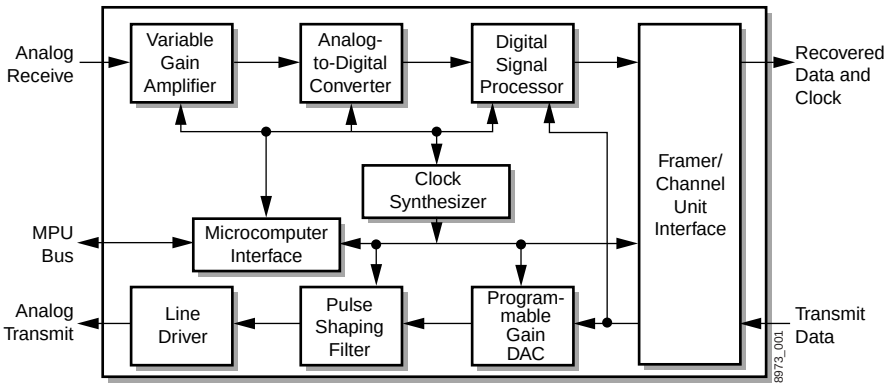
In the transmitter, the transmit source and scrambler operation are programmable through the microcomputer interface. A highly linear digital-to-analog converter with programmable gain sets the transmission power for optimal performance. A pulse shaping filter and a low-distortion line driver generate the signal characteristics needed to drive a large range of subscriber lines at low distortion.

The integrated frequency synthesizer is ideal for variable rate SDSL applications. The RS8973 can be programmed to operate at data rates ranging from 144 kbps to 2320 kbps, using a single crystal as a reference clock source.

The RS8973 is fully compliant with standards for HDSL 2B1Q transmission. Key to variable rate applications, it can meet the PSD, output power, and pulse shape requirements, as specified in ETSI TS 101 135 (formerly ETR 152) with the same support circuit. Therefore, a single design using the RS8973 can be configured through a simple software command to operate at either 784, 1168, or 2320 kbps and will still meet these ETSI requirements. No hardware changes are required.

Startup and performance monitoring operations are controlled through the microprocessor interface. C-language source code supporting these operations is supplied under a no-fee license agreement from Conexant. The RS8973 includes a glueless interface to both Intel and Motorola microprocessors.

Functional Block Diagram



Distinguishing Features

- Supports data rates ranging from 144 kbps to 2320 kbps
- Integrated frequency synthesizer
- Meets ETSI TS 101 135 (formerly ETR 152) pulse template, output power and PSD specifications at 784, 1168 and 2320 kbps data rates, using the same external support circuit
- Meets ANSI T1/E1.4/94-006 pulse template, output power and PSD specifications at 784 kbps.
- Pin-for-pin and software compatible with Bt8970 and Bt8960
- Supports automatic rate adaptation
- Single-chip 2B1Q transceiver solution
- Low power consumption (under 685 mW at 784 kbps operation)
- Glueless interface to Motorola and Intel processors
- Flexible monitoring and control
- Backwards compatible with Bt8952, Bt8960, and Bt8970 software API commands
- ZipStartup™ available for faster link establishment
- RS8953B companion SDSL/HDSL framers available
- JTAG/IEEE Std 1149.1 compliant
- 100-pin PQFP package
- –40 °C to +85 °C operation

Applications

- Variable rate data access systems
- Data access concentrators
- E1 and T1 HDSL transport
- Internet connectivity
- Voice and/or data Pair Gain systems
- N × 64 data transport
- ISDN BRI concentrators
- Cellular base station data links
- Campus modems

Ordering Information

Model Number	Package	Operating Temperature
RS8973EPF	100-Pin Plastic Quad Flat Pack	–40 °C to +85 °C

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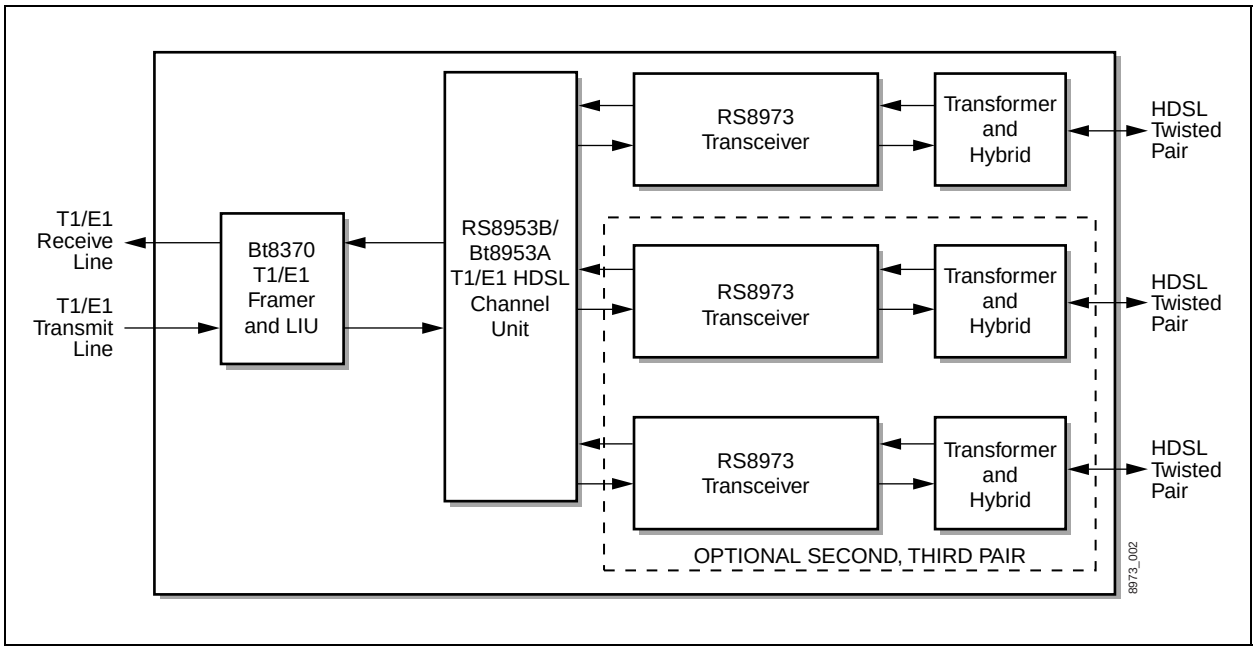
1.0 System Overview

1.1 Functional Summary

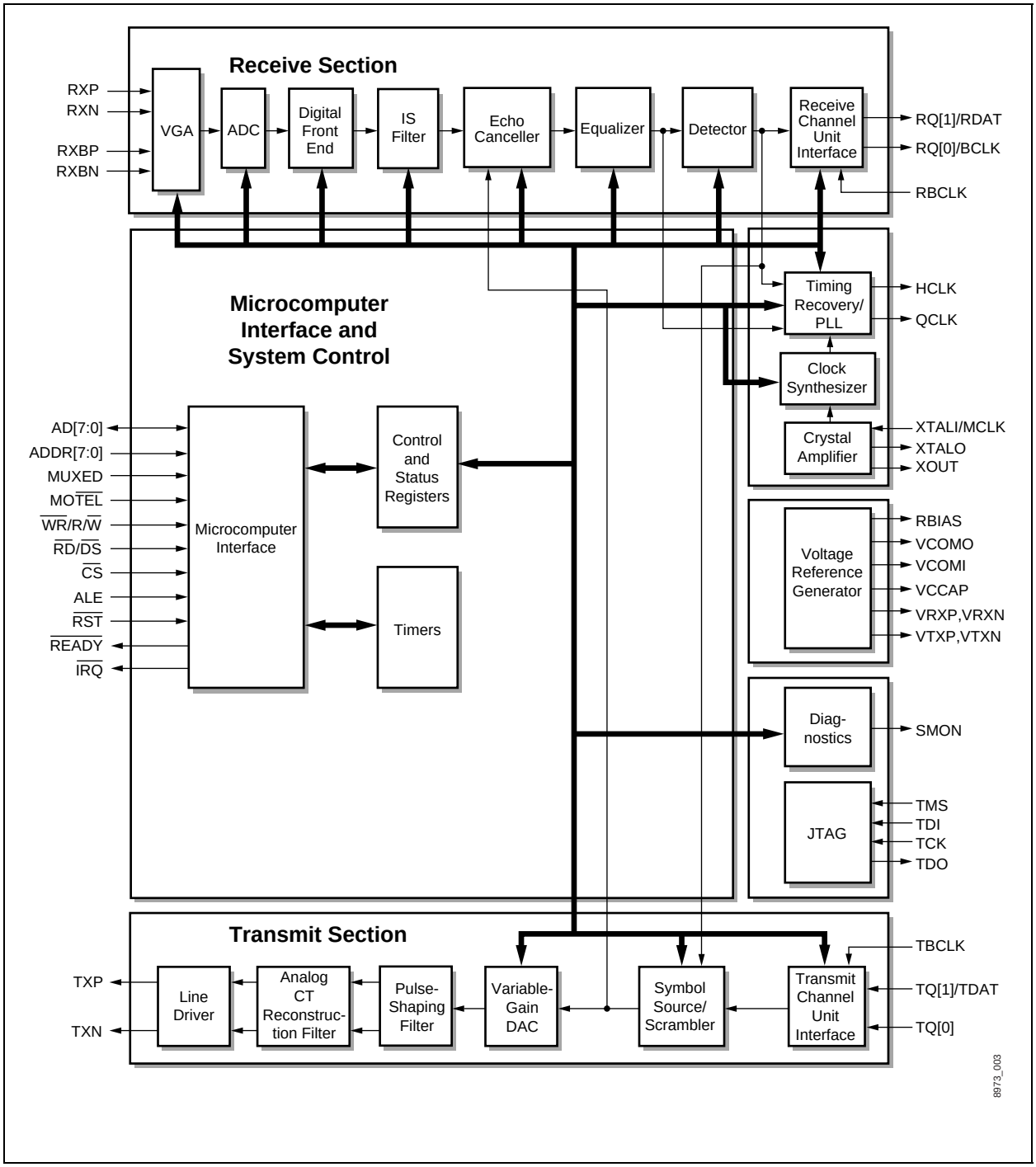
The RS8973 High-bit-rate Digital Subscriber Line (HDSL) transceiver is an integral component of Conexant's HDSL chipset. System performance of the chipset allows 2-pair T1, 1-pair E1, 2-pair E1, and 3-pair E1 transmission. With its built-in frequency synthesizer, it can easily be configured through software for variable rate Symmetric DSL over Single Pair (SDSL) applications, using a single 10.24 MHz crystal/clock as reference. It can operate at data rates between 144 kbps and 2320 kbps. The major building blocks of a typical HDSL T1/E1 terminal are shown in Figure 1-1.

Figure 1-1. HDSL T1/E1 Terminal



The RS8973 comprises five major functions: a transmit section, a receive section, a timing recovery and clock interface, a microcomputer interface, and a test and diagnostic interface. Figure 1-2 details the connections within and between each of these functional blocks.

Figure 1-2. Detailed Block Diagram



1.1.1 Transmit Section

The source of transmitted symbols is programmable through the microcomputer interface. The primary choices include external 2B1Q-encoded data presented to the TQ[1,0]/TDAT pins of the channel unit interface, internally looped-back receive symbols from the detector, or a constant “all 1s” source. The symbols are then optionally scrambled. Isolated pulses can also be generated to support the testing of pulse templates.

The digital symbols are transformed to an analog signal by means of the DAC, which is highly linear to maximize the echo cancellation and detection properties of the signal. In addition, the transmit power level of the DAC can be adjusted by means of the Transmitter Gain Register [tx_gain; 0x29] to optimize performance. The Transmitter Calibration Register [tx_calibrate; 0x28] contains the nominal setting for the transmitter gain, which is calibrated and hard-coded at the factory. The pulse-shaping filters, along with the analog continuous time (CT) reconstruction filter, then condition the signal to minimize crosstalk to adjacent subscriber lines. This filtering enables the output signal to meet requirements of ETSI TS 101 135 (formerly ETR 152) specifications for pulse shape, power spectral density and output power at 784 kbps, 1168 kbps, and 2320 kbps without any changes required to external components, including the line transformer. Finally, the differential line driver provides the current driving capabilities and low-distortion characteristics needed to drive a large range of subscriber lines.

1.1.2 Receive Section

The differential variable gain amplifier (VGA) receives the data from the subscriber line. Balancing inputs (RXBP, RXBN) are provided to accommodate first-order transmit echo cancellation through an external hybrid. The gain is programmable so that the dynamic range of the analog-to-digital converter (ADC) can be utilized according to the attenuation of the subscriber line.

Digitized receive data is passed to the digital signal processor (DSP) portion of the RS8973. After DC offset cancellation, the impulse shortening (IS) filter eliminates long tails caused by the line transformer. A replica of the transmit signal is subtracted from the total receive signal by a digital echo canceller. The resultant far-end signal is then conditioned by an equalization stage consisting of automatic gain control (AGC), a feed-forward equalizer, a decision-feedback equalizer, and an error predictor. A mode-dependent detector is then used to recover the 2B1Q-encoded data from the equalized signal. The channel unit interface then provides an optional descrambling function, followed by parallel or serial output of the sign, and magnitude bits on pins RQ[1,0]/RDAT. A number of meters are implemented within the receiver to provide average level indications at various points in the receive signal path. The receive section also performs remote unit clock recovery through an on-chip phase lock loop (PLL) circuit.

1.1.3 Timing Recovery and Clock Interface

The clock interface includes a crystal amplifier and a clock synthesizer module to reduce the external components needed for clock generation. The crystal frequency should be 10.24 MHz.

The Clock Synthesizer generates the required internal clock from this reference clock based on the data rate, as specified by the Clock Frequency Select Register [clk_select [7:0]; 0x20] and PLL Modes Register [clk_select [9,8]; 0x22]. When configured as a remote unit, the PLL module recovers the incoming data clock and outputs it on the QCLK pin (on the BCLK pin for serial mode operation). The HCLK output, which is synchronized to the QCLK signal, can be configured to cycle at 16, 32, or 64 times the symbol rate.

1.1.4 Microcomputer Interface

The microcomputer interface (MCI) provides access to a 256-byte address space within the transceiver. A combination of direct and indirect addressing methods are used to access all internal locations. The MCI is designed to interface with both Intel- and Motorola-style processors with no additional glue logic. A MO$\overline{\text{TEL}}$ control pin is provided to configure the bus interface control/handshake lines to conform to common Motorola/Intel conventions. A MUXED control pin is provided to configure the bus interface address and data lines for multiplexed or independent data/address bus operation. Little-endian data formatting (least significant byte of a multibyte word stored at the lowest byte-address location) is used in all cases, regardless of MO$\overline{\text{TEL}}$ pin selection. A $\overline{\text{READY}}$ control pin is provided to support wait-state insertion. An Interrupt Request ($\overline{\text{IRQ}}$) output pin supports low-latency responses to time-critical events within the transceiver.

Eight 16-bit timers and 10 measurement meters are integrated into the transceiver. The timers support various metering functions within the receiver section and off-load the external microcomputer from complex timing operations associated with startup procedures. Control and monitoring access to the timers and meters is provided through the MCI.

1.1.5 Test and Diagnostic Interface (JTAG)

The test and diagnostic interface comprises a test access port and a serial monitor output (SMON). The test access port conforms to IEEE Std 1149.1-1990, *(IEEE Standard Test Access Port and Boundary Scan Architecture).* Also referred to as JTAG, this interface provides direct serial access to each of the transceiver's I/O pins. This capability can be used during an in-circuit board test to increase the testability and reduce the cost of the in-circuit test process.

The serial monitor output can be viewed as a real-time virtual probe for looking at the transceiver's internal signals. The programmable signal source is shifted out serially at 16 times the symbol rate. Most of the receive signal path is accessible through this output.

1.2 Pin Descriptions

The RS8973 is packaged in a 100-pin plastic quad flat pack (PQFP). The pin assignments are shown in Figure 1-3. Pin labels, numbers, and I/O assignments are listed in Table 1-1.

Figure 1-3. Pin Diagram

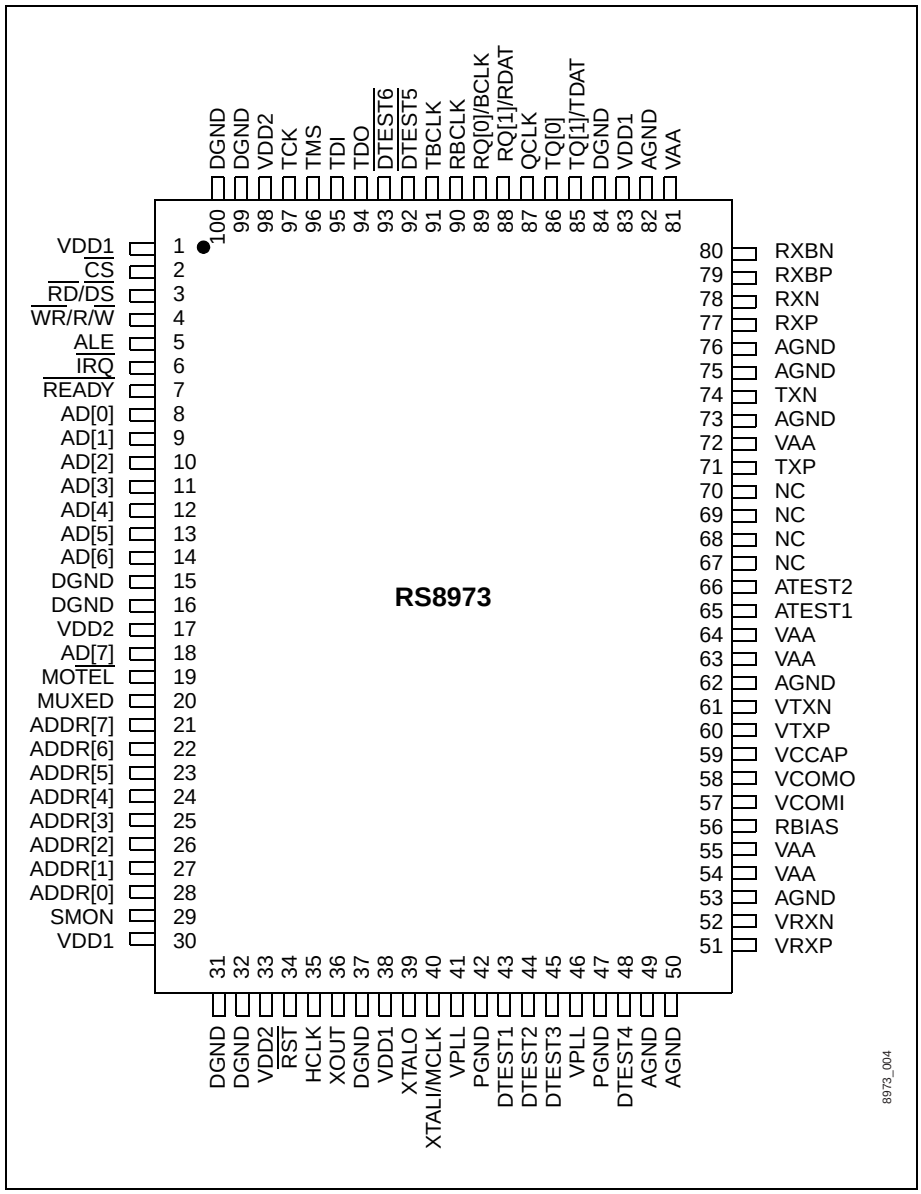


Table 1-1. Pin Descriptions

Pin	Pin Label	I/O	Pin	Pin Label	I/O	Pin	Pin Label	I/O	Pin	Pin Label	I/O
1	VDD1	–	26	ADDR[2]	I	51	VRXP	OA	76	AGND	–
2	$\overline{CS}$	I	27	ADDR[1]	I	52	VRXN	OA	77	RXP	IA
3	$\overline{RD}/\overline{DS}$	I	28	ADDR[0]	I	53	AGND	–	78	RXN	IA
4	$\overline{WR}$/R/$\overline{W}$	I	29	SMON	O	54	VAA	–	79	RXBP	IA
5	ALE	I	30	VDD1	–	55	VAA	–	80	RXBN	IA
6	$\overline{IRQ}$	OD	31	DGND	–	56	RBIAS	OA	81	VAA	–
7	$\overline{READY}$	OD	32	DGND	–	57	VCOMI	OA	82	AGND	–
8	AD[0]	I/O	33	VDD2	–	58	VCOMO	OA	83	VDD1	–
9	AD[1]	I/O	34	$\overline{RST}$	I	59	VCCAP	OA	84	DGND	–
10	AD[2]	I/O	35	HCLK	O	60	VTXP	OA	85	TQ[1]/TDAT	I
11	AD[3]	I/O	36	XOUT	O	61	VTXN	OA	86	TQ[0]	I
12	AD[4]	I/O	37	DGND	–	62	AGND	–	87	QCLK	O
13	AD[5]	I/O	38	VDD1	–	63	VAA	–	88	RQ[1]/RDAT	O
14	AD[6]	I/O	39	XTALO	O	64	VAA	–	89	RQ[0]/BCLK	O
15	DGND	–	40	XTALI/MCLK	I	65	ATEST1	IA	90	RBCLK	I
16	DGND	–	41	VPLL	–	66	ATEST2	IA	91	TBCLK	I
17	VDD2	–	42	PGND	–	67	NC	OA	92	$\overline{DTEST5}$	I
18	AD[7]	I/O	43	DTEST1	I	68	NC	OA	93	$\overline{DTEST6}$	I
19	MO$\overline{TEL}$	I	44	DTEST2	I	69	NC	IA	94	TDO	O
20	MUXED	I	45	DTEST3	I	70	NC	IA	95	TDI	I
21	ADDR[7]	I	46	VPLL	–	71	TXP	OA	96	TMS	I
22	ADDR[6]	I	47	PGND	–	72	VAA	–	97	TCK	I
23	ADDR[5]	I	48	DTEST4	I	73	AGND	–	98	VDD2	–
24	ADDR[4]	I	49	AGND	–	74	TXN	OA	99	DGND	–
25	ADDR[3]	I	50	AGND	–	75	AGND	–	100	DGND	–

Signal definitions are provided in Table 1-2. This is the coding used in the I/O column:

O = digital output
OA = analog output
OD = open-drain output
I = digital input
IA = analog input
I/O = bidirectional
NC = no connect

Table 1-2. Hardware Signal Definitions *(1 of 4)*

Pin Label	Signal Name	I/O	Definition
Microcomputer Interface (MCI)			
MOTEL	Motorola/Intel	I	Selects between Motorola and Intel handshake conventions for the RD/DS and WR/R/W signals. MOTEL = 1 for Motorola protocol: DS, R/W MOTEL = 0 for Intel protocol: RD, WR
ALE	Address Latch Enable	I	Falling-edge-sensitive input. The value of AD[7:0] when MUXED = 1, or ADDR[7:0] when MUXED = 0, is internally latched on the falling edge of ALE.
CS	Chip Select	I	Active-low input used to enable read/write operations on the MCI.
RD/DS	Read/Data Strobe	I	Bimodal input for controlling read/write access on the MCI. When MOTEL = 1 and CS = 0, RD/DS behaves as an active-low data strobe DS. Internal data is output on AD[7:0] when DS = 0 and R/W = 1. External data is internally latched from AD[7:0] on the rising edge of DS when R/W = 0. When MOTEL = 0 and CS = 0, RD/DS behaves as an active-low read strobe RD. Internal data is output on AD[7:0] when RD = 0. Write operations are not controlled by RD in this mode.
WR / R/W	Write/ Read/Write	I	Bimodal input for controlling read/write access on the MCI. When MOTEL = 1 and CS = 0, WR/R/W behaves as a read/write select line R/W. Internal data is output on AD[7:0] when DS = 0 and R/W = 1. External data is internally latched from AD[7:0] on the rising edge of DS when R/W = 0. When MOTEL = 0 and CS = 0, WR/R/W behaves as an active-low write strobe WR. External data is internally latched from AD[7:0] on the rising edge of WR. Read operations are not controlled by WR in this mode.
AD[7:0]	Address-Data[7:0]	I/O	An 8-bit, bidirectional multiplexed address-data bus. AD[7] = MSB, AD[0] = LSB. Usage is controlled using MUXED.
ADDR[7:0]	Address Bus (not multiplexed)[7:0]	I	Provides a glueless interface to microcomputers with separate address and data buses. ADDR[7] = MSB, ADDR[0] = LSB. Usage is controlled using MUXED.
MUXED	Addressing Mode Select	I	Controls the MCI addressing mode. When MUXED = 1, the MCI uses AD[7:0] as a multiplexed signal for address and data. When MUXED = 0, the MCI uses ADDR[7:0] as the address input, and AD[7:0] for data only.
READY	Ready	OD	Active-low, open-drain output that indicates the MCI is ready to transfer data. Can be used to signal the microcomputer to insert wait states.
IRQ	Interrupt Request	OD	Active-low, open-drain output that indicates requests for interrupt. Asserted whenever at least one unmasked interrupt flag is set. Remains inactive whenever no unmasked interrupt flags are present.

Table 1-2. Hardware Signal Definitions *(2 of 4)*

Pin Label	Signal Name	I/O	Definition
$\overline{\text{RST}}$	Reset	I	Asynchronous, active-low, level-sensitive input that places the transceiver in an inactive state by setting the power-down mode bit of the Global Modes and Status Register [global_modes; 0x00], and zeroing the clk_freq [7:0] bits of the Clock Frequency Select Register [clock_freq;0x20], clk_freq[9,8] bits of the PLL Modes Register [pll_modes; 0x22], and the hclk_freq[1,0] bits of the Serial Monitor Source Select Register [serial_monitor_source; 0x01]. All RAM contents are lost. Does not affect the state of the test access port, which is reset automatically at power-up only.
			Channel Unit Interface
RQ[1]/ RDAT RQ[0]/ BCLK	Receive Quat 1/ Receive Data Receive Quat 0/ Bit Clock	O O	RQ[1]/RDAT and RQ[0]/BCLK are bimodal outputs that represent the sign and magnitude bits of the received quaternary output symbol in parallel channel unit modes (RQ[1], RQ[0]), and the serial-data and bit-clock outputs in serial channel unit modes (RDAT, BCLK). Behavior of these outputs is configurable through the Channel Unit Interface Modes Register [CU_interface_modes; 0x06] for parallel master, parallel slave, serial magnitude-bit-first, and serial sign-bit-first operations. For parallel mode operation: RQ[1] = Sign bit output RQ[0] = Magnitude bit output Both outputs are updated at the symbol rate on the rising edge of QCLK (master mode) or the rising/falling edge (programmable) of RBCLK (slave mode). For serial mode operation: RDAT = Serial quaternary data output BCLK = Bit-rate (two times symbol rate) clock output RDAT is updated at the bit rate on the rising edge of BCLK
TQ[1]/ TDAT TQ[0]	Transmit Quat 1/ Transmit Data Transmit Quat 0	I I	TQ[1]/TDAT and TQ[0] are bimodal inputs that represent the sign and magnitude bits of the quaternary input symbol to be transmitted in parallel channel unit modes (TQ[1], TQ[0]), and the serial data input in serial channel unit modes (TDAT). Interpretation of these inputs is configurable through the Channel Unit Interface Modes Register [CU_Interface_modes; 0x06] for parallel master, parallel slave, serial magnitude-bit-first and serial sign-bit-first operations. For parallel mode operation: TQ[1] = Sign bit input TQ[0] = Magnitude bit input Both inputs are sampled at the symbol rate on the falling edge of QCLK (master mode) or the rising/falling edge (programmable) of TBCLK (slave mode). For serial mode operation: TDAT = Serial quaternary data input TQ0 = Don't care (tie or pull up to supply rail) TDAT is sampled at the bit rate (two times the symbol rate) on the falling edge of BCLK.
QCLK	Quaternary Clock	O	Runs at the symbol rate. It defines the data on the TQ and RQ interfaces. QCLK is also used to frame transmit/receive quats in serial mode.

Table 1-2. Hardware Signal Definitions *(3 of 4)*

Pin Label	Signal Name	I/O	Definition
TBCLK	Transmit Baud-Rate Clock	I	Functions as the transmit baud-rate clock input. It must be frequency-locked to QCLK. This input is used only when the channel unit interface is in parallel slave mode. If it is unused, it should be tied to VDD2 or DGND.
RBCLK	Receive Baud-Rate Clock	I	Functions as the receive baud-rate clock input. It must be frequency-locked to QCLK. This input is used only when the channel unit interface is in parallel slave mode. If it is unused, it should be tied to VDD2 or DGND.
Analog Transmit Interface			
TXP, TXN	Transmit Positive, Negative	OA	Differential transmit line driver outputs. These signals are used to drive the subscriber line after passing through the hybrid and line transformer.
Analog Receive Interface			
RXP, RXN	Receive Positive, Negative	IA	Differential receiver inputs. RXP and RXN receive the signal from the subscriber line.
RXBP, RXBN	Receive Balance Positive, Negative	IA	Differential receiver balance inputs. RXBP and RXBN are used to subtract the echo of the signal being transmitted on the subscriber line. They should be connected to the TXP, TXN output pins through the hybrid circuit. This signal is subtracted from the signal being received by the RXP and RXN inputs in the VGA.
Voltage Reference Generator Interface			
RBIAS	Resistor Bias	OA	Connection point for external bias resistor.
VCOMO	Common Mode Voltage Outputs	OA	Common mode voltage for the analog circuitry. This pin should be connected to an external filtering capacitor.
VCOMI	Common Mode Voltage Inputs	OA	Common mode voltage for the analog circuitry. This pin should be connected to an external filtering capacitor.
VCCAP	Voltage Compensation Capacitor	OA	Analog voltage compensation capacitor. This pin should be connected to an external filtering capacitor.
VRXP, VRXN	Receiver Voltage Reference Positive, Negative	OA	Analog receive circuitry reference voltages. These pins should be connected to external filtering capacitors.
VTXP, VTXN	Transmit Voltage Reference Positive, Negative	OA	Analog transmit circuitry reference voltages. These pins should be connected to external filtering capacitors.
Clock Interface			
XTALI/ MCLK	Crystal In/Master Clock	I	A bimodal input that can be used as the crystal input or as the master clock input. The frequency of the crystal or clock should be 10.24 MHz.
XTALO	Crystal Output	O	Connection point for the crystal. If an external clock is connected to XTALI/MCLK, XTALO should be left floating.
HCLK	High Speed Clock Out	O	HCLK can be configured to run at 16, 32, or 64 times the symbol rate. Upon reset, it is set to 16 times the symbol rate. This clock will be phase locked to the incoming data when the RS8973 is configured as the remote unit.
XOUT	Crystal Clock Out	O	Buffered-crystal oscillator output.

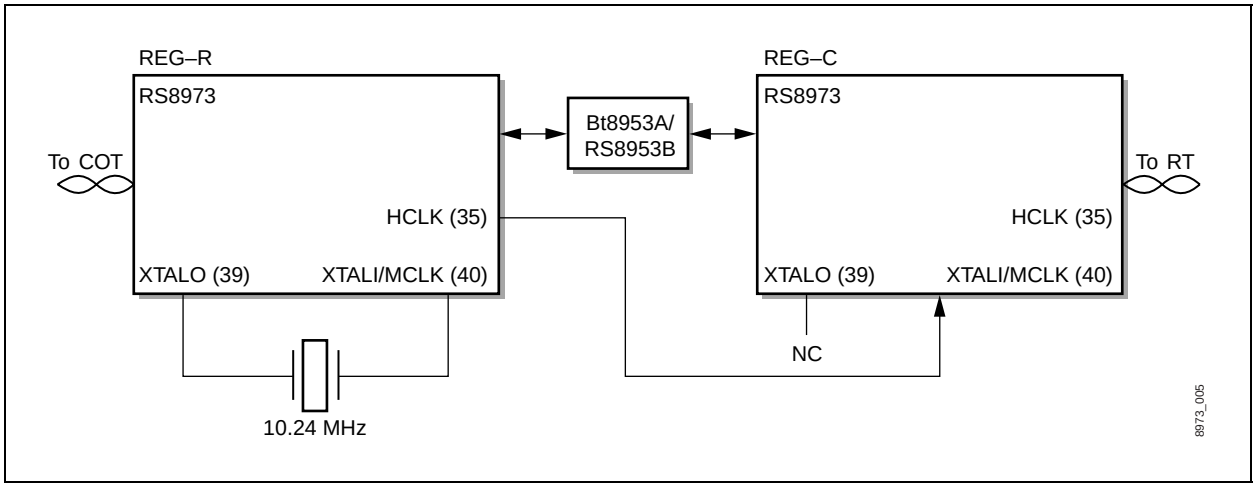
Table 1-2. Hardware Signal Definitions *(4 of 4)*

Pin Label	Signal Name	I/O	Definition
Test and Diagnostic Interface			
TDI	JTAG Test Data Input	I	JTAG test data input per IEEE Std 1149.1-1990. Used for loading all serial instructions and data into internal test logic. Sampled on the rising edge of TCK. TDI can be left unconnected if it is not being used because it is pulled up internally.
TMS	JTAG Test Mode Select	I	JTAG test mode select input per IEEE Std 1149.1-1990. Internally pulled-up input signal used to control the test-logic state machine. Sampled on the rising edge of TCK. TMS can be left unconnected if it is not being used because it is pulled up internally.
TDO	JTAG Test Data Output	O	JTAG test data output per IEEE Std 1149.1-1990. Three-state output used for reading all serial configuration and test data from internal test logic. Updated on the falling edge of TCK.
TCK	JTAG Test Clock Input	I	JTAG test clock input per IEEE Std 1149.1-1990. Used for all test interface and internal test logic operations. If unused, TCK should be pulled low.
SMON	Serial Monitor	O	Serial data output used for real-time monitoring of internal signal-path registers. The source register is selected through the Serial Monitor Source Select Register [serial_monitor_source; 0x01]. The 16-bit words are shifted out, LSB first, at 16 times the symbol rate. The rising edge of QCLK defines the start LSB of each word. The output is updated on the rising edge of an internal clock running at 16 times QCLK.
DTEST[1:4]	Digital Tests 1–4	I	Active-high test inputs used by Conexant to enable internal test modes. These inputs should be tied to digital ground (DGND).
$\overline{\text{DTEST[5, 6]}}$	Digital Test 5, 6	I	Active-low test inputs used by Conexant to enable internal test modes. These inputs should be tied to the I/O buffer power supply (VDD2).
ATEST[1,2]	Analog Test 1, 2	IA	Analog test inputs used by Conexant for internal test modes. These inputs should be left floating (No Connect, NC).
Power and Ground			
VDD1	Core Logic Power Supply	–	Dedicated supply pins powering the digital core logic functions. Connect to 3.3 V.
VDD2	I/O Buffer Power Supply	–	Dedicated supply pins powering the digital I/O buffers. Connect to 5 V.
VPLL	PLL Power Supply	–	Dedicated supply pins powering the PLL and the crystal amplifier. Connect to 5 V.
PGND	PLL Ground	–	Dedicated ground pins for the PLL and the crystal amplifier. Must be held at the same potential as DGND and AGND.
DGND	Digital Ground	–	Dedicated ground pins for the digital circuitry. Must be held at same potential as AGND and PGND.
VAA	Analog Power Supply	–	Dedicated supply pins powering the analog circuitry.
AGND	Analog Ground	–	Dedicated ground pins for the analog circuitry. Must be held at the same potential as DGND and PGND.

1.3 Regenerator Configuration

Figure 1-4 shows the interconnection between two RS8973s for a single loop regenerator system. Bt8953A/RS8953B provides an internal cross-connect data path between REG-R and REG-C.

Figure 1-4. Regenerator System Block Diagram



HCLK on REG–R is configured to run at 16 times the symbol rate, which is the power-on default.

The reg_clk_en bit of Miscellaneous/Test Register (0x0F) is reset (0) on REG–R.

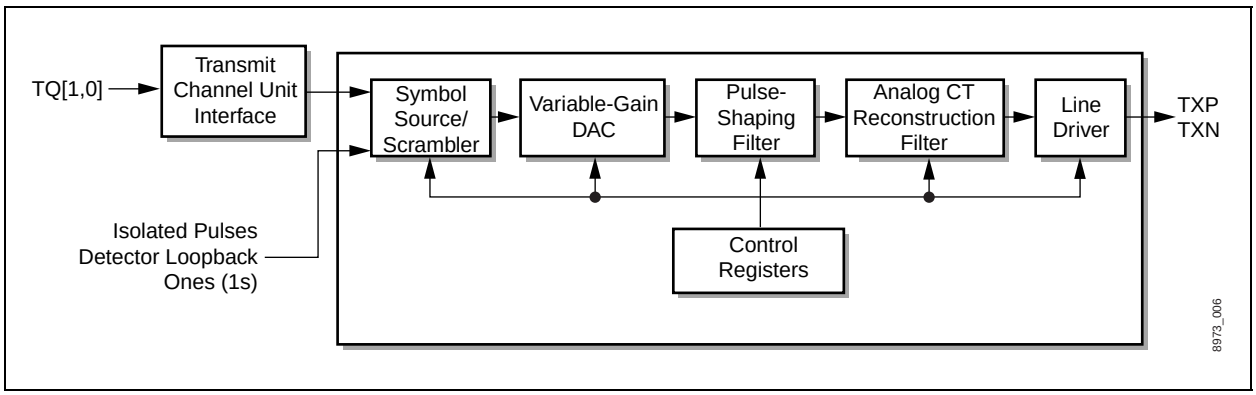
The reg_clk_en bit of Miscellaneous/Test Register (0x0F) is set (1) on REG–C. In this mode, the internal clock synthesizer is bypassed.

2.0 Functional Description

2.1 Transmit Section

The transmit section block diagram is shown in Figure 2-1. It comprises five major functions: a symbol source selector/scrambler, a variable gain digital-to-analog converter (DAC), a pulse-shaping filter, an analog CT reconstruction filter, and a line driver.

Figure 2-1. Transmit Section Block Diagram



2.1.1 Symbol Source Selector/Scrambler

The input source selector/scrambler can be configured through the Transmitter Modes Register [transmitter_modes; 0x0B] data_source [2:0] bits. It selects the source of the data to be transmitted and determines whether the data is scrambled. The symbol source selector/scrambler modes are described in Table 2-1.

Table 2-1. Symbol Source Selector/Scrambler Modes

data_source[2:0]	Symbol Source Selector/Scrambler Mode
000	Isolated pulse. Level selected by isolated_pulse[1,0]. The meter timer must be enabled and in continuous mode. The pulse repetition interval is determined by the meter timer countdown interval.
001	Four-level scrambled detector loopback. Sign and magnitude bits from the receiver detector are scrambled and looped back to the transmitter. Feedback polynomial determined by the htur_lfsr control bit.
010	Four-level unscrambled data. Transmits the four-level (2B1Q) sign and magnitude bits from the transmit channel unit transmit interface without scrambling.
011	Four-level scrambled 1s. Transmits a scrambled, constant high-logic level as a four-level (2B1Q) signal. Feedback polynomial determined by the htur_lfsr control bit.
100	Alternating symbol mode. Outputs symbols of alternating polarity. Level is selected by isolated_pulse [1:0]. The meter timer must be enabled and in continuous mode. The half period of the output signal is defined by the meter timer countdown interval.
101	Four-level scrambled data. Scrambles and transmits the four-level (2B1Q) sign and magnitude bits from the channel unit transmit interface. Feedback polynomial determined by the htur_lfsr control bit.
110	Two-level unscrambled data. Constantly forces the magnitude bit from the transmit channel unit interface to a logic 0, and transmits the resulting two-level signal (as determined by the sign bit) without scrambling. Valid output levels are limited to + 3 and – 3.
111	Two-level scrambled 1s. Transmits a scrambled, constant high-logic level as a two-level signal. Feedback polynomial determined by the htur_lfsr control bit. Scrambler is run at the symbol rate (half-bit rate) to produce the sign bit of the transmitted signal, while the magnitude bit is sourced with a constant logic 0. Valid output levels are limited to + 3 and – 3.

The bit stream is converted into symbols for the four-level cases, as shown in Table 2-2.

Table 2-2. Four-Level Bit-to-Symbol Conversions

First Input Bit (Sign)	Second Input Bit (Magnitude)	Output Symbol
0	0	– 3
0	1	– 1
1	1	+ 1
1	0	+ 3

In two-level mode, the magnitude bit is forced to a 0. This forces the symbols to be + 3 and – 3, as shown in Table 2-3.

Table 2-3. Two-Level Bit-to-Symbol Conversions

First Input Bit (Sign)	Second Input Bit (Magnitude)	Output Symbol
0	Don't Care	– 3
1	Don't Care	+ 3

The scrambler is essentially a 23-bit-long Linear Feedback Shift Register (LFSR). The feedback points are programmable for central office and remote terminal applications using the htur_lfsr bit of the Transmitter Modes Register. The LFSR polynomials for local (HTU-C/LTU) and remote (HTU-R/NTU) unit operations are:

$$local \Rightarrow x^{-23} \oplus x^{-5} \oplus 1$$
$$remote \Rightarrow x^{-23} \oplus x^{-18} \oplus 1$$

The scrambler operates differently depending on whether a two-level or four-level mode is specified. In two-level scrambled-1s mode, the LFSR is clocked once per symbol; in four-level mode, the LFSR is clocked twice per symbol.

The Transmitter Modes Register can also be used to zero the output of the transmitter using the transmitter_off control bit.

The RS8973 can generate isolated pulses to support the testing of pulse templates. When in the isolated pulse mode, the output consists of a single pulse surrounded by 0s.

NOTE: Zero is not a valid 2B1Q level and occurs only in this special mode or when the transmitter is off. The repetition rate of the pulses is controlled by the meter timer. Any of the four 2B1Q levels can be chosen through the Transmitter Modes Register's isolated_pulse[1,0] control bits.

2.1.2 Variable Gain Digital-to-Analog Converter

A four-level DAC is integrated into the RS8973 to convert the output of the symbol source to analog form. The normalized values of these four analog levels are + 3, + 1, – 1 and – 3. Each represents a symbol, or quat.

To provide precise adjustment of transmitted power, the level of the DAC can be adjusted. The Transmitter Gain Register [tx_gain; 0x29] sets the level.

During the manufacturing of the RS8973, process variations can cause changes in transmitter levels. The Transmitter Calibration Register [tx_calibrate; 0x28] contains a read-only value which nulls this variation. The value in this register is determined for each RS8973 device during production testing. Upon initialization, the Transmitter Gain Register should be loaded based on the Transmitter Calibration Register.

If there are other sources of transmit power variation (e.g., a nonstandard hybrid or attenuative lightening protection), the transmitter gain must be adjusted to include these effects. The range of adjustment of the transmitter gain is from – 1.60 dB to 1.40 dB.

2.1.3 Pulse-Shaping Filter

The pulse-shaping filter is used to filter the quats output from the variable-gain DAC. This filter, when combined with other filtering in the signal path, produces a transmitted signal on the line that meets the power spectral density, the transmitted power, and the pulse-shaping requirements, as specified in Chapter 5.0, *Electrical and Mechanical Specifications*.

2.1.4 Analog CT Reconstruction Filter

The analog CT reconstruction filter removes the discrete-time images from the transmit signal before it is amplified by the line driver.

2.1.5 Line Driver

The line driver buffers the output of the CT reconstruction filter to drive diverse loads. The output of the line driver is differential.

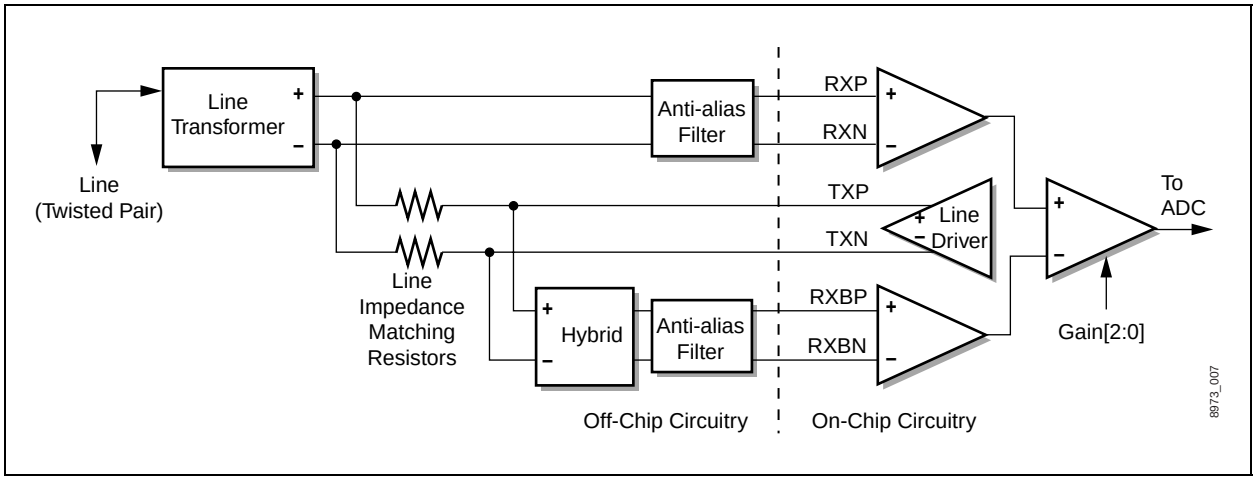
2.2 Receive Section

Like the transmit section, the receive section consists of both analog and digital circuitry. The VGA provides the interface to the analog signals received from the line and the hybrid. The ADC then digitizes the analog signal so it can be further processed in the DSP section of the receiver. The receiver DSP section includes front-end processing, echo cancellation, equalization, and symbol detection.

2.2.1 Variable Gain Amplifier

The VGA has two purposes. The first is to provide a dual-differential analog input so the pseudo-transmit signal created by the hybrid can be subtracted from the signal received from the line transformer. This subtraction provides first-order echo cancellation, which results in a first-order approximation of the signal received from the line. Figure 2-2 illustrates the recommended echo-cancellation circuit interconnections. All off-chip circuitry, including the hybrid and anti-alias filters, consists entirely of passive components. Further echo cancellation occurs in the receiver DSP.

Figure 2-2. First-Order Echo Cancellation Using the Variable Gain Amplifier



The second purpose of the VGA is to provide programmable gain of the received signal prior to passing it to the ADC. This reduces the resolution required for the ADC. There are six gain settings ranging from 0 dB to 15 dB (this is the gain setting range in relative terms; the physical settings range from – 3 dB to 12 dB). The gain is controlled through the gain[2:0] control bits in the ADC Control Register [adc_control; 0x21]. See Chapter 3.0, *Registers*, for a more detailed description of the gain[2:0] control bits.

2.2.2 Analog-to-Digital Converter

The ADC provides 16 bits of resolution. The analog input from the variable gain amplifier is converted into digital data and output at the symbol rate.

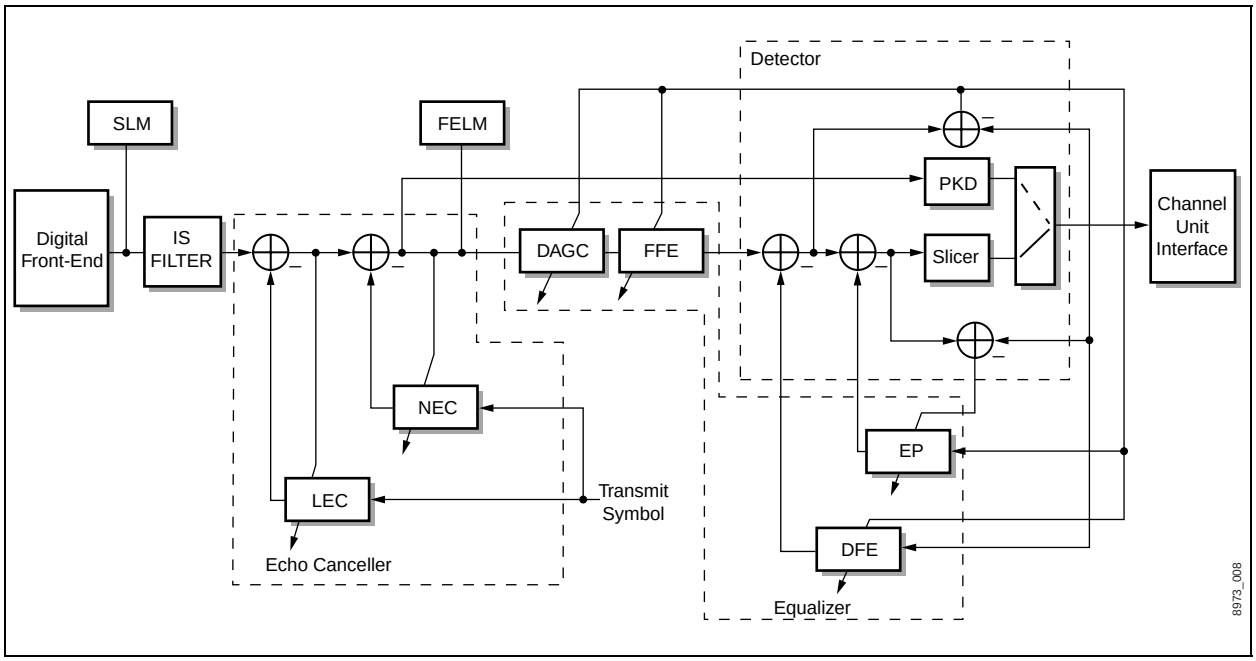
2.2.3 Digital Signal Processor

The DSP includes five Least Mean Squared (LMS) filters:

- Echo Canceller (EC)
- Digital Automatic Gain Controller (DAGC)
- Feed Forward Equalizer (FFE)
- Error Predictor (EP)
- Decision Feedback Equalizer (DFE).

These filters are used to equalize the received signal so that the symbols transmitted from the far-end can be reliably recovered. The DSP uses symbol rate sampling for all processing functions. Figure 2-3 shows the interconnections and relationships to the digital front-end and the detector.

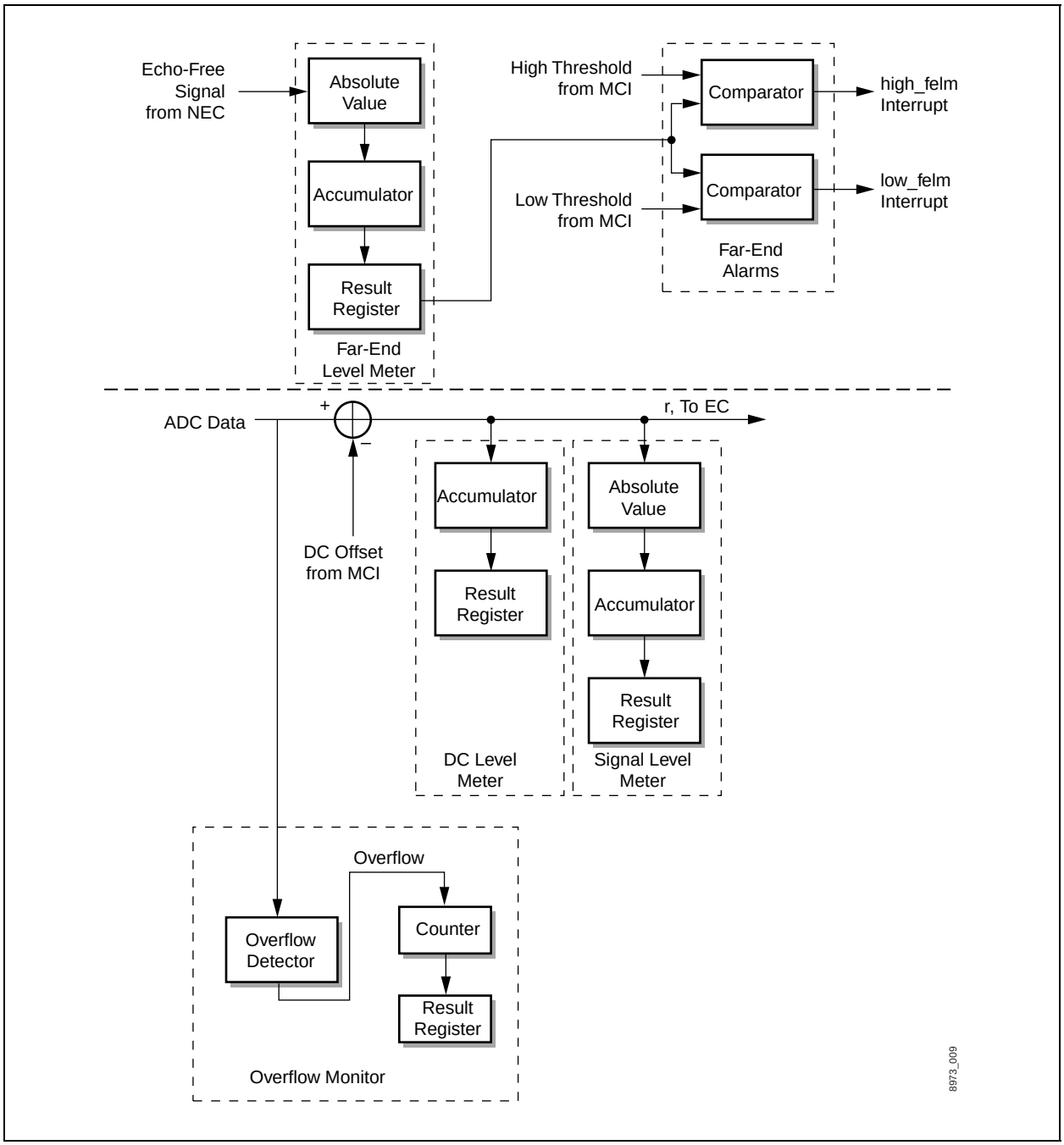
Figure 2-3. Receiver Digital Signal Processing



2.2.3.1 Digital Front-End

Prior to the main signal processing, the input signal must be adjusted for any DC offset. The front-end module also monitors the input signal level, which includes measuring DC and AC input signal levels, detecting and counting overflows, and detecting alarms based on the far-end signal level. Figure 2-4 summarizes the features of the digital front-end module.

Figure 2-4. Digital Front-End Block Diagram



2.2.3.2 Offset Adjustment

A nonzero DC level on the input can be corrected by a DC offset value [dc_offset_low, dc_offset_high; 0x26, 0x27], which is subtracted from the input. The DC offset is a 16-bit number and is programmed through the microcomputer interface.

2.2.3.3 DC Level Meter

The DC level meter provides the monitoring needed for adaptive offset compensation. The offset-adjusted input signal is accumulated over the meter timer interval [meter_low, meter_high; 0x18, 0x19]. The 16 MSBs are placed into the DC Level Meter Registers [dc_meter_low, dc_meter_high; 0x44, 0x45].

2.2.3.4 Signal Level Meter

The Signal Level Meter provides the monitoring needed for adjusting the analog gain circuit located before the ADC. The absolute value of the offset adjusted input signal is accumulated over the meter timer interval [meter_low, meter_high; 0x18, 0x19]. The 16 MSBs are placed in the Signal Level Meter Registers [slm_low, slm_high; 1; 0x46, 0x47].

2.2.3.5 Overflow Detection and Monitoring

The overflow sensor detects ADC overflows. The overflow monitor counts the number of overflows, as indicated by the overflow sensor during the meter timer interval [meter_low, meter_high; 0x18, 0x19]. The counter is limited to 8 bits. In the case of 256 or more overflows during the measurement interval, the counter will hold at 255. The counter is loaded into the Overflow Meter Register [overflow_meter; 0x42] at the end of each measurement interval.

2.2.3.6 Far-End Level Meter

The Far-end Level Meter monitors the output of the echo canceller, which is called the far-end signal because the echo of the transmitted signal is subtracted from it. This value is accumulated over the meter timer interval [meter_low, meter_high; 0x18, 0x19]. The 16 MSBs are placed into the Far-End Level Meter Register [felm_low, felm_high; 0x48, 0x49].

2.2.3.7 Far-End Level Alarm

The result of the far-end level meter is compared to two thresholds. When these are exceeded, an interrupt is sent to the microcomputer interface if the corresponding FELM interrupt is enabled. The thresholds are determined by the value in the Far-End High Alarm Threshold Registers [far_end_high_alarm_th_low, far_end_high_alarm_th_high; 0x30, 0x31] and the Far-End Low Alarm Threshold Registers [far_end_low_alarm_th_low, far_end_low_alarm_th_high; 0x32, 0x33].

The interrupts high_felm and low_felm are bits 2 and 1, respectively, of the IRQ Source Register [irq_source; 0x05]. The interrupts high_felm and low_felm can be masked by writing a 1 to bits 2 and 1, respectively, of the Interrupt Mask Register High [mask_high_reg; 0x03].

2.2.4 Impulse Shortening Filter

The impulse shortening (IS) filter is a high pass filter which pre-equalizes the channel and eliminates long tails caused by the transformer.

2.2.5 Echo Canceller

The echo canceller (EC) removes images of the transmitted symbols from the received signal and consists of two blocks: a linear and nonlinear echo canceller. The organization of the blocks is displayed in Figure 2-3, *Receiver Digital Signal Processing*.

2.2.5.1 Linear Echo Canceller

The linear echo canceller (LEC) is a conventional LMS, finite impulse response (FIR) filter, which removes linear images of the transmitted symbols from the received signal. It consists of a 120-tap FIR filter with 32-bit adapted coefficients.

When LEC is enabled, the last data tap of the echo canceller is treated specially; the data value is set to a constant 1. This serves to cancel any DC offset that may be present.

These modes, used less often, can also be enabled through the MCI:

- A freeze coefficient mode disables the coefficient updates.
- A special mode zeros all of the coefficients.
- An additional mode zeros the output of the FIR with no effect on the coefficients.
- Individual EC coefficients can be read and written through the MCI.

2.2.5.2 Nonlinear Echo Canceller (NEC)

The nonlinear echo canceller (NEC) reduces the residual echo power in the echo canceller output caused by nonlinear effects in the transmitter, receiver, analog hybrid circuitry, or line cables.

The delay of the transmit-symbol input to the NEC can be specified through the MCI, Nonlinear Echo Canceller Mode Register [nonlinear_ec_modes; 0x09]. This allows the NEC to operate on the peak of the echo regardless of differing delays in the echo path.

These modes, used less often, can also be enabled through the MCI:

- A freeze coefficient mode disables the coefficient updates.
- A special mode zeros all of the coefficients.
- An additional mode zeros the output of the look-up table with no effect on the coefficients.
- The 64 14-bit, individual NEC coefficients can be read and written through the MCI.

2.2.6 Equalizer

Four LMS filters are used in the equalizer to process the echo canceller output so that received symbols can be reliably recovered. The filters are a digital automatic gain controller, a feed forward equalizer, an error predictor, and a decision feedback equalizer. Their interconnections are shown in Figure 2-3, *Receiver Digital Signal Processing*.

2.2.6.1 Digital Automatic Gain Control

The digital automatic gain control (DAGC) scales the echo-free signal to the optimum magnitude for subsequent processing.

Two other modes, used less often, can also be enabled through the MCI:

- A freeze coefficient mode disables the coefficient update.
- The DAGC gain coefficient can be read or written through the MCI.

2.2.6.2 Feed Forward Equalizer

The feed forward equalizer (FFE) removes precursors from the received signal. The FFE can be operated in a special *adapt last* mode. In this mode, which is useful during startup, only the last coefficient is updated. The last coefficient is multiplied with the oldest data sample (sample #7).

Other modes, used less often, can be enabled through the MCI:

- A freeze coefficient mode disables the coefficient updates.
- A special mode zeros all of the coefficients.
- Individual FFE coefficients can be read and written through the MCI.

2.2.6.3 Error Predictor

The error predictor (EP) improves the performance of the equalizer by prognosticating errors before they occur.

Other modes, used less often, can be enabled through the MCI:

- A freeze coefficient mode disables the coefficient updates.
- A special mode zeros all of the coefficients.
- Individual EP coefficients can be read and written through the MCI.

2.2.6.4 Decision Feedback Equalizer

The decision feedback equalizer (DFE) removes postcursors from the received signal.

Other modes, used less often, can be enabled through the MCI:

- A freeze coefficient mode disables the coefficient updates.
- A zero coefficients mode zeros all of the coefficients.
- A zero filter output mode zeros the output of the FIR with no effect on the coefficients.
- Individual DFE coefficients can be read and written through the MCI.

2.2.6.5 Microcoding

The DAGC, FFE, and EP filters are implemented using an internal microprogrammable DSP, optimized for LMS filters. Internal DSP micro-instructions are stored in an on-chip RAM. This microcode RAM is loaded after power-up through the MCI when the transceiver is initialized.

2.2.7 Detector

The detector converts the equalized received signal into a 2B1Q symbol and produces two error signals used in adapting the receiver equalizers. The signal detection uses two sub-blocks, a slicer, and a peak detector. Additionally, the detector contains a scrambler and bit error rate (BER) meter for use during the start-up sequence.

2.2.7.1 Slicer

The slicer thresholds the equalized signal to produce a 2B1Q symbol. The input to the slicer is the FFE output minus the DFE and EP outputs.

The slicer can operate in two modes: two-level and four-level. In the two-level mode, which is used during start-up when the only transmitted symbols are + 3 or – 3, the slicer threshold is set at zero.

In the four-level mode, the cursor level is specified through the MCI. It is a 16-bit, 2s complement number, but must be positive and less than 0x2AAA for proper operation.

2.2.7.2 Peak Detector

The peak detector (PKD) is used only during the two-level transmission part of start-up. It operates on the echo-free signal. A signal is detected to be a + 3 if it is higher than both of its neighbors, or a – 3 if it is lower than both of its neighbors. If neither of the peaked conditions exist, the output of the slicer is used.

2.2.7.3 Error Signals

The detector computes two error signals for use in the equalizer: a 16-bit slicer and a 16-bit equalizer.

2.2.7.4 Scrambler Module

The scrambler can operate as either a scrambler or as a descrambler. The scrambler block is used during the scrambled-1s part of the start-up sequence. This provides an error-free signal for equalizer adaptation. This scrambler is essentially a 23-bit-long Linear Feedback Shift Register (LFSR). The feedback point depends on whether the transceiver is being used in a central-office or remote-terminal application.

When the LFSR is operating as a descrambler, the input source is the detector output. The symbol is converted to a bit stream as shown in Table 2-4 for the two-level case.

Table 2-4. Two-Level Symbol-to-Bit Conversion

Input Symbol	Output Bit
– 3	0
+ 3	1

The symbol is converted to a bit stream as shown in Table 2-5 for the four-level case.

Table 2-5. Four-Level Symbol-to-Bit Conversion

Input Symbol	First Output Bit (Sign)	Second Output Bit (Magnitude)
– 3	0	0
– 1	0	1
+ 1	1	1
+ 3	1	0

The LFSR operates in the same way in both cases, except that in the two-level case it is clocked once per symbol, and in the four-level case it is clocked twice per symbol.

When operating as a scrambler, the LFSR must first be locked to the far-end source. Once locked, it is then able to replicate the far-end input sequence when its input is held at all 1s. The locking sequence is controlled internally, initiated through the MCI by setting the lfsr_lock bit of the detector_modes register. The locking sequence consists of the following four steps:

1. Operate the LFSR as a *descrambler* for 23 bits.
2. Operate the LFSR as a *scrambler* for 127 bits. The sync detector is active during this period.
3. Go to Step 1 if synchronization was not achieved; otherwise, continue to Step 4.
4. Send an interrupt to the microcomputer if unmasked, indicating successful locking, and continue operating as a scrambler.

The sequence continues until the lfsr_lock control bit is cleared by the microcomputer.

2.2.7.5 Sync Detector

The sync detector compares the output of the scrambler with the output of the symbol detector. The number of equivalent bits is accumulated for 128 comparisons. The result is then compared to a Scrambler Synchronization Threshold Register [scr_sync_th; 0x2E], a lock is declared, and the sync bit of the irq_source register is set if the count is greater than the threshold. For a count less than or equal to the threshold, no lock condition is declared and the sync bit is unaffected.

2.2.7.6 Detector Meters

The detector consists of five meters: a BER meter, a symbol histogrammer, a noise-level meter, a noise-level histogram meter, and an SNR alarm meter.

BER Meter

The BER meter provides an estimate of the bit error rate when the received symbols are known to be scrambled 1s. When the LFSR is operating as a descrambler, the meter counts the number of 1s on the descrambler output. When the LFSR is operating as a scrambler, the BER meter counts the number of equal scrambler and symbol detector outputs. The counter operates over the meter timer interval [meter_low, meter_high; 0x18, 0x19]. The counter is saturated to 16 bits. At the end of the measurement interval the counter is loaded into the Bit Error Rate Meter Registers [ber_meter_low, ber_meter_high; 0x4C, 0x4D].

Symbol Histogrammer

The symbol histogrammer computes a coarse histogram of the received symbols. It operates by counting the number of 1s received during the meter timer interval [meter_low, meter_high; 0x18, 0x19]. That is, at the start of the measurement interval a counter is cleared. For each detector output which is + 1 or – 1, the counter is incremented. If the detector output is + 3 or – 3, the count is held at its previous value. The count is saturated to 16 bits. At the end of the measurement interval, the 8 MSBs of the counter are loaded into the Symbol Histogram Meter Register [symbol_histogram; 0x4E]. This can be used during start-up to detect the transition from two-level to four-level signalling.

Noise Level Meter

The noise level meter estimates the noise at the input to the slicer. It operates by accumulating the absolute value of the slicer error over meter timer interval [meter_low, meter_high; 0x18, 0x19]. At the end of the measurement interval, the 16 MSBs of the 32-bit accumulator are loaded into the Noise Level Meter Register [nlm_low, nlm_high; 0x50, 0x51].

Noise Level Histogram Meter

The noise level histogram meter counts the number of high noise-level conditions which occur during each meter countdown interval. A high noise-level condition is defined as the absolute value of the slicer error signal exceeding the threshold specified in the noise level histogram threshold register [0x2A,2B].

SNR Alarm

The SNR alarm provides a rapid indication of impulse noise disturbances and loss of signal so that corrective action can be taken. The alarm is based on a second noise level meter. The meter is the same as the preceding noise level meter except it operates on a dedicated timer, the SNR alarm timer. The absolute value of the slicer error is accumulated during the timer period. At the end of the measurement interval, the 16 MSBs of the accumulator are compared against the SNR Alarm Threshold Register [snr_alarm_th_low, snr_alarm_th_high; 0x34, 0x35]. If the result is greater than this threshold, an interrupt is set in the irq_source register. The threshold is set through the MCI.

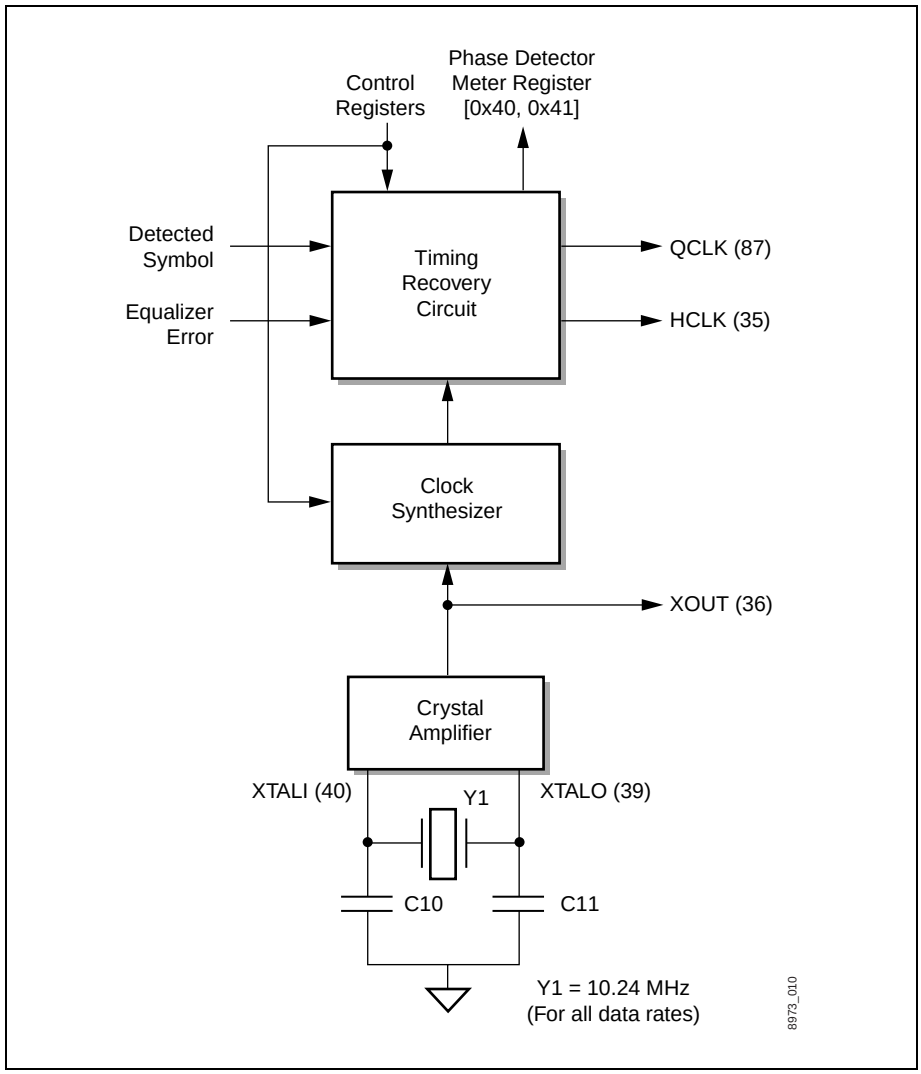
2.3 Timing Recovery and Clock Interface

The timing recovery and clock interface block consists of the timing recovery circuit, the crystal amplifier, and the clock synthesizer, as detailed in Figure 2-5. The main purpose of this circuitry is to generate the internal clocks, including BCLK and QCLK, from the 10.24 MHz input MCLK, based on the selected data rate, and to recover the clock from received data. Control fields include the following:

- Clock Frequency Select Register [clk_select; 0x20]
- PLL Modes Register [clk_select; 0x22]
- hclk_freq[1,0] bits of the Serial Monitor Source Select Register [serial_monitor_source; 0x01]
- PLL Modes Register [pll_modes; 0x22]
- Timing Recovery PLL Phase Offset Register [pll_phase_offsset_low, pll_phase_offset_high; 0x24, 0x25]
- PLL Frequency Register [pll_frequency_low, pll_frequency_high; 0x5E, 0x5F].

See Chapter 3.0, *Registers*, for descriptions of these control fields.

Figure 2-5. Timing Recovery and Clock Interface Block Diagram



2.3.1 Timing Recovery Circuit

The timing recovery circuit uses the RS8973's internal detected symbol and equalizer error signals to regenerate the received data symbol clock (QCLK). The HCLK output is synchronized with the edges of the symbol clock (QCLK), unlike the XOUT output, which is a buffered output of the crystal amplifier. HCLK can be programmed for rates of 16, 32, or 64 times the symbol rate.

The timing recovery circuit includes a phase detector meter that measures the average value of a phase correction signal. This information can be used during start-up to set the phase offset in the Receive Phase Select Register [receive_phase_select; 0x07]. The output of the phase detector is accumulated over the meter timer interval [meter_low, meter_high; 0x18, 0x19]. At the end of the measurement interval, the value is loaded into the Phase Detector Meter Register [pdm_low, pdm_high; 0x40, 0x41].

The user can also bypass the timing recovery circuit and directly specify the frequency through the PLL Frequency Register [pll_frequency_low, pll_frequency_high; 0x5E, 0x5F].

2.3.2 Crystal Amplifier

The crystal amplifier reduces the support circuitry needed for the RS8973 by eliminating the need for an external crystal oscillator (XO). A crystal of 10.24 MHz frequency can be connected directly to the XTALI and XTALO pins. The crystal amplifier can also accommodate an external clock input by connecting the external clock to the XTALI input pin.

2.3.3 Clock Synthesizer

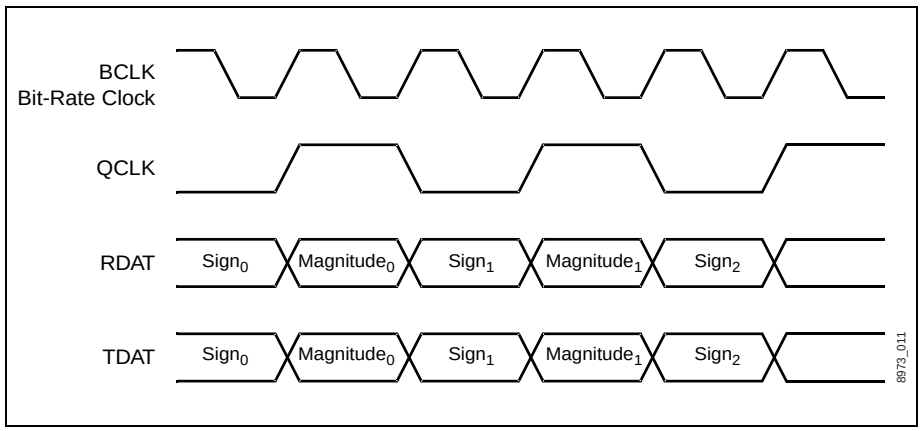
The clock synthesizer takes the 10.24 MHz input clock as a reference and generates internal clocks required for data rates ranging from 144 kbps to 2320 kbps. The appropriate internal clock frequency can be selected by specifying the data rate in the Clock Frequency Select Register [clk_select [7:0]; 0x20] and PLL Modes Register [clk_select [9,8]; 0x22].

2.4 Channel Unit Interface

The quaternary signals of the channel unit interface have four modes which are programmable through bits 0 and 1 of the Channel Unit Interface Modes Register [cu_interface_modes; 0x06]. They are serial sign-bit first, serial magnitude-bit first, parallel master, and parallel slave.

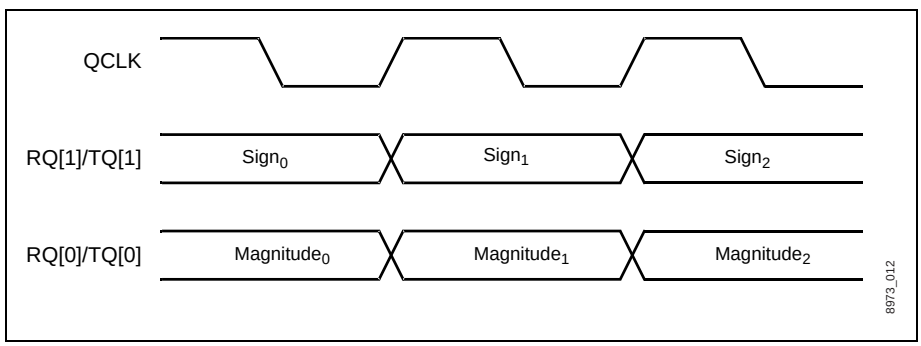
In serial mode, a Bit-Rate Clock (BCLK) is output at twice the symbol rate. The sign and magnitude bits of the receive data are output through RDAT on the rising edge of BCLK. The sign and magnitude bits of the transmit data are sampled on the falling edge of BCLK at the TDAT input. The sign bit is transferred first, followed by the magnitude bit of a given symbol in sign-bit first mode, while the opposite occurs in magnitude-bit first mode. The clock relationships for serial sign-bit first mode are illustrated in Figure 2-6.

Figure 2-6. Serial Sign-Bit First Mode



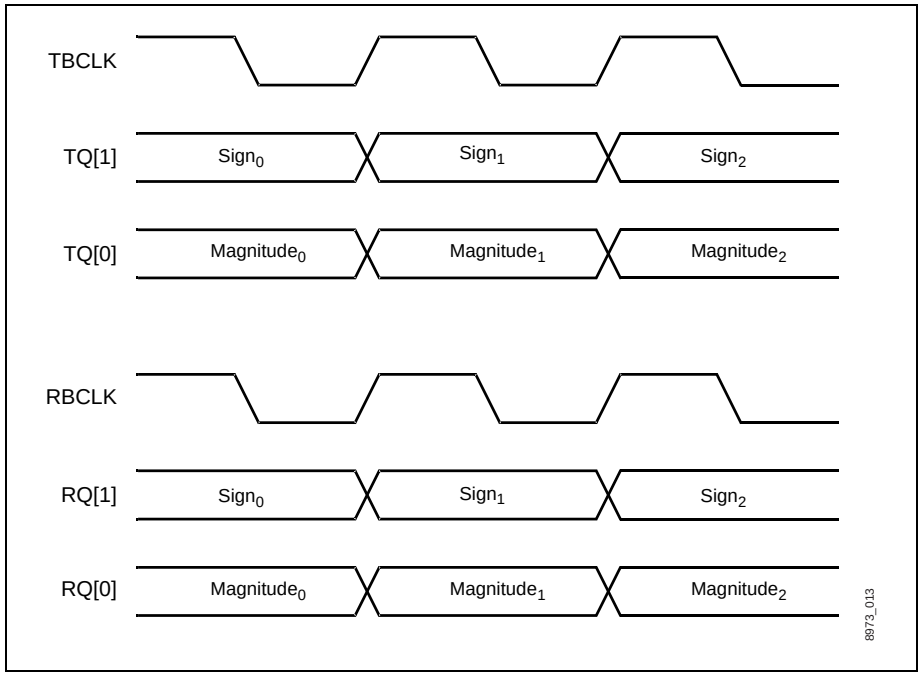
In parallel master mode, the sign and magnitude receive data is output through RQ[1] and RQ[0], respectively, on the rising edge of QCLK. The quaternary transmit data is sampled on the falling edge of QCLK. This clock and data relationship is illustrated in Figure 2-7.

Figure 2-7. Parallel Master Mode



The parallel slave mode uses RBCLK and TBCLK inputs to synchronize data transfer. RBCLK and TBCLK must be frequency-locked to QCLK, though the use of two internal FIFOs allows an arbitrary phase relationship to QCLK. TQ[1] and TQ[0] are sampled on the active edge of TBCLK, as programmed through the MCI. RQ[1] and RQ[0] are output on the active edge of RBCLK, also as programmed through the MCI. Figure 2-8 shows the clock relationships, when TBCLK is programmed to be falling-edge active and RBCLK is rising-edge active.

Figure 2-8. Parallel Slave Mode



2.5 Microcomputer Interface

The microcomputer interface provides operational mode control and status through internal registers. A microcomputer write sets the operating modes to the appropriate registers. A read to a register verifies the operating mode or provides the status. The MCI can be programmed to generate an interrupt on certain conditions.

2.5.1 Source Code

Conexant provides portable C-source code under a no-cost licensing agreement. This source code provides a start-up procedure, as well as diagnostic and system monitoring functions.

2.5.2 Microcomputer Read/Write

The MCI uses either an 8-bit-wide multiplexed address-data bus, or an 8-bit-wide data bus and a separate 8-bit-wide address bus for external data communications. The interface provides access to the internal control and status registers, coefficients, and microcode RAM. The interface is compatible with Intel or Motorola microcomputers, and is configured with the inputs, MO$\overline{\text{TEL}}$ and MUXED.

- MO$\overline{\text{TEL}}$ high selects Motorola-type microcomputer and uses control signals ALE, $\overline{\text{CS}}$, $\overline{\text{DS}}$, and R/$\overline{\text{W}}$. MO$\overline{\text{TEL}}$ low selects Intel-type microcomputer and uses control signals ALE, $\overline{\text{CS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$.
- MUXED high configures the interface to use the multiplexed address-data bus with both the address and data on the AD[7:0] pins. MUXED low configures the interface to use separate address and data bus with the data on the AD[7:0] pins and the address on the ADDR[7:0] pins.
- The $\overline{\text{READY}}$ pin is provided to indicate when the RS8973 is ready to transfer data and can be used by the microcomputer to insert wait states in read or write cycles.

The MCI provides access to a 256-byte internal address space. The registers in this address space provide configuration, control, status, and monitoring capabilities.

Meter values are read lower-byte, then upper-byte. When the lower-byte is read, the upper-byte is latched at the corresponding value. This ensures that multiple byte values correspond to the same reading.

Most information can be directly read or written; however, the filter coefficients require an indirect access.

2.5.2.1 RAM Access Registers

The internal RAM of the scratch pad, LEC, NEC, DFE, equalizer, and microcode are accessed indirectly. They all share a common data register which is used for both read and write operations: Access Data Register [access_data_byte[3:0]; [0x7C–0x7F]. Each RAM has an individual read select and write select register. Writes to these registers specify the location to access and trigger the actual RAM read or write.

To perform a read, the address of the desired RAM location is first written to the corresponding read tap select register. Two symbol periods afterward, the individual bytes of that location are available for reading from the Access Data Register.

To perform a write, the value to be written is first stored in the Access Data Register. The address of the affected RAM location is then written to the corresponding write tap select register. When writing the same value to multiple locations, it is not necessary to rewrite the Access Data Register.

To ensure reliable access to the embedded RAM, internal read and write operations are performed synchronous to the symbol clock. This limits access to the internal RAM to one every other cycle.

When reading or writing multiple filter coefficients, it may be desirable to freeze adaptation so that all values correspond to the same state.

2.5.2.2 Multiplexed Address/Data Bus

The timing for a read or write cycle is stated explicitly in Chapter 5.0, *Electrical and Mechanical Specifications*. During a read operation, an external microcomputer places an address on the address-data bus, which is then latched on the falling edge of ALE. Data are placed on the address-data bus after $\overline{CS}$ and $\overline{RD}$, or $\overline{CS}$ and $\overline{DS}$ go low. The read cycle is completed with the rising edge of $\overline{CS}$ or $\overline{RD}$ or $\overline{DS}$.

A write operation latches the address from the address-data bus at the falling edge of ALE. The microcomputer places data on the address-data bus after $\overline{CS}$, and $\overline{WR}$ or $\overline{CS}$ and $\overline{DS}$ go low. Motorola MCI has R/$\overline{W}$ falling edge preceding the falling edge of $\overline{CS}$ and $\overline{DS}$. The rising edge of R/$\overline{W}$ occurs after the rising edge of $\overline{CS}$ and $\overline{DS}$. Data are latched from the address-data bus on the rising edge of $\overline{CS}$ or $\overline{WR}$ or $\overline{DS}$.

2.5.2.3 Separated Address/ Data Bus

The timing for a read or write cycle using the separated address and data buses is essentially the same as over the multiplexed bus. The one exception is that the address must be driven onto the ADDR[7:0] bus rather than the AD[7:0] bus.

2.5.3 Interrupt Request

The 12 interrupt sources consist of 8 timers, a far-end signal high alarm, a far-end signal low alarm, a SNR alarm, and a scrambler synchronization detector. All of the interrupts are requested on a common pin, $\overline{IRQ}$. Each interrupt can be individually enabled or disabled through the Interrupt Mask Registers [mask_low_reg, mask_high_reg; 0x02, 0x03]. The cause of an interrupt is determined by reading the Timer Source Register [timer_source; 0x04] and the IRQ Source Register [irq_source; 0x05].

The timer interrupt status is set only when the timer transitions to zero. Alarm interrupts cannot be cleared while the alarm is active. In other words, it cannot be cleared while the condition still exists.

$\overline{IRQ}$ is an open-drain output and must be tied to a pull-up resistor. This allows $\overline{IRQ}$ to be tied to a common interrupt request.

2.5.4 Reset

The reset input ($\overline{RST}$) is an active-low input that places the transceiver in an inactive state by setting the mode bit (0) in the Global Modes and Status Register [global_modes; 0x00]. An internal supply monitor circuit ensures that the transceiver is in an inactive state upon initial application of power to the chip.

2.5.5 Registers

The RS8973 has many directly addressable registers that include control and monitoring functions. Write operations to undefined registers have unpredictable effects. Read operations from undefined registers have undefined results.

2.5.6 Timers

Eight timers are integrated into the RS8973 to control the various on-chip meters and to aid the microcomputer in stepping through the events of the start-up sequence.

The structure of each timer includes down counter, zero detect logic, and control circuitry, which determines when the counter is reloaded or decremented.

For each of the 8 timers, there is a 2-byte timer interval register that determines the value from which the timer decrements. There are three 8-bit registers:

- Timer Restart Register [timer_restart; 0x0C]
- Timer Enable Register [timer_enable; 0x0D]
- Timer Continuous Mode Register [timer_continuous; 0x0E].

These registers control the operation of the timers. Each bit of the 8-bit registers corresponds to a timer. Each logic-high bit in timer_restart acts as an event that causes the corresponding timer to reload. Each logic-high bit in timer_enable acts to enable the corresponding timer. Each logic-high bit in timer_continuous acts to reload the counter after timing out.

Each counter is loaded with the value in its interval register. The counter decrements until it reaches zero. Upon reaching zero, an interrupt is generated if enabled by the Interrupt Mask Low Register [mask_low_reg, mask_high_reg; 0x02, 0x03]. The interrupt is edge-triggered so that only one interrupt is caused by a single time-out.

A prescaler can precede the timer. This increases the time span available at the expense of resolution. Only the start-up timers have prescalers. Table 2-6 provides summary information on the timers.

Table 2-6. Timers

Timer Name	Purpose	Clock Rate	Control Bits
Startup Timer 1	Startup Events	Symbol rate ÷ 1024	sut 1
Startup Timer 2	Startup Events	Symbol rate ÷ 1024	sut 2
Startup Timer 3	Startup Events	Symbol rate ÷ 1024	sut 3
Startup Timer 4	Startup Events	Symbol rate ÷ 1024	sut 4
SNR Alarm Timer	SNR Measurement	Symbol rate	snr
Meter Timer	Measurement	Symbol rate	meter
General Purpose Timer 3	Miscellaneous	Symbol rate	t3
General Purpose Timer 4	Miscellaneous	Symbol rate	t4

Four timers are provided for use in timing start-up events. These timers share a single prescaler, which divides the symbol clock by 1024 and supplies this slow clock to the four counters. The timers are Startup Timer 1, Startup Timer 2, Startup Timer 3, and Startup Timer 4. Each one is independent, with separate interval timer values and interrupts.

Two timers control the measurement intervals for the various meters: the SNR Alarm Timer and the Meter Timer. The SNR Alarm Timer is used only by the low SNR, while the Meter Timer is used by all other meters, excluding the low SNR meter. Their respective interrupts are set when each of these two timers expires. There are no prescalers for these timers; they count at the symbol rate. Both timers are normally used in the continuous mode.

Two identical timers are provided for general use: General Purpose Timer 3 and General Purpose Timer 4. There are no prescalers for these timers; they count at the symbol rate. Each timer signals an interrupt when it expires.

2.5.7 Scratch Pad Memory

The scratch pad memory consists of 64 bytes of RAM available to the external microcomputer. This is used by Conexant-supplied software to minimize system memory requirements.

2.6 Test and Diagnostic Interface (JTAG)

To access individual chips for PCB verification, special circuitry is incorporated within the transceiver, which complies with *IEEE Std 1149.1-1990, Standard Test Access Port and Boundary Scan Architecture* set by the Joint Test Action Group (JTAG).

JTAG has four dedicated pins that comprise the test access port (TAP):

1. Test Mode Select (TMS)
2. Test Clock (TCK)
3. Test Data Input (TDI)
4. Test Data Out (TDO)

Verification of the integrated circuit's connection to other modules on the printed circuit board can be achieved through these four TAP pins.

JTAG's approach to testability uses boundary scan cells placed at each digital pin, both inputs and outputs. All scan cells are interconnected in a boundary-scan register which applies or captures test data used for functional verification of the PC board interconnection. JTAG is particularly useful for board testers using functional testing methods.

The boundary-scan cells at each digital pin provide the ability to apply and capture the respective logic levels. Since all of the digital pins are interconnected as a long shift register, the TAP logic has access and control of all necessary pins to verify connectivity. For mixed signal ICs, the chip boundary definition is expanded to include the on-chip interface between digital and analog circuitry. During a power-up sequence, internal supply-monitor circuitry ensures that each pin is initialized to operate as a 2B1Q transceiver, instead of JTAG test mode.

The JTAG standard defines an optional device identification register. This register is included and contains a revision number, a part number, and a manufacturer's identification code specific to Conexant (see Table 2-7). Access to this register is through the TAP controller through a standard JTAG instruction.

A variety of verification procedures can be performed through the TAP controller. Board connectivity can be verified at all digital pins through a set of two instructions accessible through the use of a state machine, standard to all JTAG controllers. Refer to the IEEE Std 1149.1 specification for details concerning the Instruction Register and JTAG state machine. A Boundary Scan Description Language (BSDL) file for the RS8973 is also available from the factory upon request.

Table 2-7. JTAG Device Identification Register

Version(1)	Part Number	Manufacturer ID	
0 0 0 0	0 0 1 0 0 0 1 1 0 0 0 0 1 1 0 1	0 0 0 1 1 0 1 0 1 1 0 1	TDO
0x0	0x230D (RS8973)	0x0D6	
4 bits	16 bits	11 bits	

NOTE(S):
(1) Consult factory for current version number.

3.0 Registers

3.1 Conventions

Unless otherwise noted, the following conventions apply to all applicable register descriptions:

- For storage of multiple-bit data fields within a single byte-wide register, the LSBs of the field are located at the lower register-bit positions, whereas the MSBs are located at the higher positions.
- If only a single data field is stored in a byte-wide register, the field is justified so that the LSB of the field is located in the lowest register-bit position, bit 0.
- For storage of multiple-byte data words across multiple byte-wide registers, the LSBs of the word are located at the lower byte-address locations, while the MSBs are located at the higher byte-address locations.
- When writing to any control or data register with less than all 8-bit positions defined, a logical 0 value must be assigned to each unused/undefined/reserved position. Writing a logical 1 value to any of these positions may cause undefined behavior.
- When reading from any control/status or data register with less than all 8-bit positions defined, an indeterminate value is returned from each unused/undefined/reserved position.
- Register values are not affected by $\overline{\text{RST}}$ pin assertion, except for the mode bit of the Global Modes and Status Register [global_modes; 0x00], the hclk_freq[1,0] field of the Serial Monitor Source Select Register [serial_monitor_source; 0x01] and the clk_freq[1,0] field of the PLL Modes Register [pll_modes; 0x22]. After $\overline{\text{RST}}$ pin assertion, all device parameters should be reinitialized.
- The initial values of all registers and RAM are undefined after power is applied. Exceptions include the mode bit of the Global Modes and Status Register, the hclk_freq[1,0] field of the Serial Monitor Source Select Register, the clk_freq[9,8] field of PLL Modes Register, and the Clock Frequency Select Register. In addition, the JTAG state is reset when power is applied.
- The register and bit mnemonics used here are based on the mnemonics used in the Conexant bit pump software.
- Writing to unspecified registers may cause unpredictable behavior.

3.2 Register Summary

Table 3-1 displays a summary of the registers.

Table 3-1. Register Table *(1 of 5)*

ADDR (Hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
0x00	global_modes	R/W	hw_revision[3]	hw_revision[2]	hw_revision[1]	hw_revision[0]	part_id[2]	part_id[1]	part_id[0]	mode
0x01	serial_monitor_source	R/W	hclk_freq[1]	hclk_freq[0]	smon[5]	smon[4]	smon[3]	smon[2]	smon[1]	smon[0]
0x02	mask_low_reg	R/W	t4	t3	snr	meter	sut4	sut3	sut2	sut1
0x03	mask_high_reg	R/W	—	—	—	—	sync	high_felm	low_felm	low_snr
0x04	timer_source	R/W	t4	t3	snr	meter	sut4	sut3	sut2	sut1
0x05	irq_source	R/W	—	—	—	—	sync	high_felm	low_felm	low_snr
0x06	cu_interface_modes	R/W	—	—	—	tbclk_pol	rbclk_pol	fifos_mode	interface_mode1	interface_mode[0]
0x07	receive_phase_select	R/W	—	imp_short[2]	imp_short[1]	imp_short[0]	rphs[3]	rphs[2]	rphs[1]	rphs[0]
0x08	linear_ec_modes	R/W	—	—	enable_dc_tap	adapt_coefficients	zero_coefficients	zero_output	adapt_gain[1]	adapt_gain[0]
0x09	nonlinear_ec_modes	R/W	negate_symbol	symbol_delay[2]	symbol_delay[1]	symbol_delay[0]	adapt_coefficients	zero_coefficients	zero_output	adapt_gain
0x0A	dfe_modes	R/W	—	—	—	—	adapt_coefficients	zero_coefficients	zero_output	adapt_gain
0x0B	transmitter_modes	R/W	—	isolated_pulse[1]	isolated_pulse[0]	transmitter_off	htur_lfsr	data_source[2]	data_source[1]	data_source[0]
0x0C	timer_restart	R/W	t4	t3	snr	meter	sut4	sut3	sut2	sut1
0x0D	timer_enable	R/W	t4	t3	snr	meter	sut4	sut3	sut2	sut1
0x0E	timer_continuous	R/W	t4	t3	snr	meter	sut4	sut3	sut2	sut1
0x0F	misc_test	R/W	res[6]	res[5]	reg_clk_en	res[4]	res[3]	res[2]	res[1]	async_mode
0x10	sut1_low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

Table 3-1. Register Table *(2 of 5)*

ADDR (Hex)	Register Label	Read Write	Bit Number								
			7	6	5	4	3	2	1	0
0x11	sut1_high	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x12	sut2_low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x13	sut2_high	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x14	sut3_low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x15	sut3_high	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x16	sut4_low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x17	sut4_high	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x18	meter_low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x19	meter_high	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x1A	snr_timer_low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x1B	snr_timer_high	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x1C	t3_low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x1D	t3_high	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x1E	t4_low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x1F	t4_high	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x20	clock_freq_select	R/W	clk_freq[7]	clk_freq[6]	clk_freq[5]	clk_freq[4]	clk_freq[3]	clk_freq[2]	clk_freq[1]	clk_freq[0]
0x21	adc_control	R/W	cont_time[1]	cont_time[0]	loop_back[1]	loop_back[0]	switch_cap_pole	gain[2]	gain[1]	gain[0]
0x22	pll_modes	R/W	clk_freq[9]	clk_freq[8]	—	phase_detector_ gain[1]	phase_detector_ gain[0]	freeze_pll	pll_gain[1]	pll_gain[0]
0x23	test_reg23	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x24	pll_phase_offset_low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

Table 3-1. Register Table *(3 of 5)*

ADDR (Hex)	Register Label	Read Write	Bit Number									
			7	6	5	4	3	2	1	0
0x25	pll_phase_offset_high	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x26	dc_offset_low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x27	dc_offset_high	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x28	tx_calibrate	R/W	—	—	tx_calibrate[3]	tx_calibrate[2]	tx_calibrate[1]	tx_calibrate[0]	—	—
0x29	tx_gain	R/W	—	—	tx_gain[3]	tx_gain[2]	tx_gain[1]	tx_gain[0]	—	—
0x2A	noise_histogram_th_low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x2B	noise_histogram_th_high	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x2C	ep_pause_th_low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x2D	ep_pause_th_high	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x2E	scr_sync_th	R/W	—	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x30	far_end_high_alarm_th_low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x31	far_end_high_alarm_th_high	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x32	far_end_low_alarm_th_low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x33	far_end_low_alarm_th_high	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x34	snr_alarm_th_low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x35	snr_alarm_th_high	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x36	cursor_level_low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x37	cursor_level_high	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x38	dagc_target_low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x39	dagc_target_high	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]

Table 3-1. Register Table *(4 of 5)*

ADDR (Hex)	Register Label	Read Write	Bit Number								
			7	6	5	4	3	2	1	0
0x3A	detector_modes	R/W	enable_peak_detector	output_mux_control[1]	output_mux_control[0]	scr_out_to_dfe	two_level	lfsr_lock	htur_lfsr	descr_on
0x3B	peak_detector_delay	R/W	—	—	—	—	D[3]	D[2]	D[1]	D[0]
0x3C	dagc_modes	R/W	—	—	—	—	—	eq_error_adaption	adapt_coefficients	adapt_gain
0x3D	ffe_modes	R/W	—	—	—	—	adapt_last_coeff	zero_coefficients	adapt_coefficients	adapt_gain
0x3E	ep_modes	R/W	—	—	—	—	zero_output	zero_coefficients	adapt_coefficients	adapt_gain
0x40	pdm_low	R/W	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]
0x41	pdm_high	R/W	D[25]	D[24]	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]
0x42	overflow_meter	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x44	dc_meter_low	R/W	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]
0x45	dc_meter_high	R/W	D[31]	D[30]	D[29]	D[28]	D[27]	D[26]	D[25]	D[24]
0x46	slm_low	R/W	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]
0x47	slm_high	R/W	D[31]	D[30]	D[29]	D[28]	D[27]	D[26]	D[25]	D[24]
0x48	felm_low	R/W	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]
0x49	felm_high	R/W	D[31]	D[30]	D[29]	D[28]	D[27]	D[26]	D[25]	D[24]
0x4A	noise_histogram_low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x4B	noise_histogram_high	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x4C	ber_meter_low	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x4D	ber_meter_high	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x4E	symbol_histogram	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

Table 3-1. Register Table *(5 of 5)*

ADDR (Hex)	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
0x50	nlm_low	R/W	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]
0x51	nlm_high	R/W	D[31]	D[30]	D[29]	D[28]	D[27]	D[26]	D[25]	D[24]
0x5E	pll_frequency_low	R/W	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]	D[15]
0x5F	pll_frequency_high	R/W	D[30]	D[29]	D[28]	D[27]	D[26]	D[25]	D[24]	D[23]
0x70	linear_ec_tap_select_read	R/W	—	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x71	linear_ec_tap_select_write	R/W	—	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x72	nonlinear_ec_tap_select_read	R/W	—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x73	nonlinear_ec_tap_select_write	R/W	—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x74	dfe_tap_select_read	R/W	—	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x75	dfe_tap_select_write	R/W	—	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x76	sp_tap_select_read	R/W	—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x77	sp_tap_select_write	R/W	—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x78	eq_add_read	R/W	—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x79	eq_add_write	R/W	—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x7A	eq_microcode_add_read	R/W	—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x7B	eq_microcode_add_write	R/W	—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x7C	access_data_byte0	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x7D	access_data_byte1	R/W	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]
0x7E	access_data_byte2	R/W	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]
0x7F	access_data_byte3	R/W	D[31]	D[30]	D[29]	D[28]	D[27]	D[26]	D[25]	D[24]

3.3 Register Description

0x00—Global Modes and Status Register (global_modes)

7	6	5	4	3	2	1	0
hw_revision[3]	hw_revision[2]	hw_revision[1]	hw_revision[0]	part_id[2]	part_id[1]	part_id[0]	mode

hw_revision[3:0] Chip Revision Number—Read-only unsigned binary field encoded with the chip revision number. Smaller values represent earlier versions, while larger values represent later versions. The zero value represents the original prototype release. Consult factory for current values and revision.

part_id[2:0] Part ID—Read-only binary field set to binary 011, identifying the part as RS8973.

The following table shows Part IDs for different DSL transceivers:

part_id[2]	part_id[1]	part_id[0]	Device Name
0	0	0	Bt8952
0	0	1	Bt8960
0	1	0	Bt8970
0	1	1	RS8973

mode Power Down Mode—Read/write control bit. When set, stops all filter processing and zeros the transmit output for reduced power consumption. All RAM contents are preserved. The mode bit is automatically set by $\overline{\text{RST}}$ assertion and upon initial power application. It can be cleared only by writing a logic 0, at which time filter processing and transmitter operation can proceed.

0x01—Serial Monitor Source Select Register (serial_monitor_source)

7	6	5	4	3	2	1	0
hclk_freq[1]	hclk_freq[0]	smon[5]	smon[4]	smon[3]	smon[2]	smon[1]	smon[0]

hclk_freq[1,0] HCLK Frequency Select—Read/write binary field selects the frequency of the HCLK output.

hclk_freq[1]	hclk_freq[0]	HCLK Frequency
0	0	Upon assertion of the $\overline{RST}$ pin and power-on detection, hclk_freq[1,0] is set to 00. Symbol Frequency (F_{QCLK}) × 16. Upon assertion of the $\overline{RST}$ pin and power-on detection, hclk_freq[1,0] is set to 00.
0	1	Symbol Frequency (F_{QCLK}) × 16
1	0	Symbol Frequency (F_{QCLK}) × 32
1	1	Symbol Frequency (F_{QCLK}) × 64

smon[5:0] Serial Monitor Source Select—Read/write binary field selects the Serial Monitor (SMON) output source.

smon[5:0]		Source
Decimal	Binary	
0 – 47	00 0000 – 10 1111	Equalizer register file
48	11 0000	Digital front-end output/IS input
49	11 0001	Linear echo replica
50	11 0010	DFE subtractor output
51	11 0011	EP subtractor output/slicer input
52	11 0100	Timing recovery phase detector output/loop filter input
53	11 0101	Timing recovery loop filter output/frequency synthesizer input

0x02—Interrupt Mask Register Low (mask_low_reg)

Independent read/write mask bits for each of the Timer Source Register [timer_source; 0x04] interrupt flags. A logical 1 represents the masked condition. A logical 0 represents the unmasked condition. All mask bits behave identically with respect to their corresponding interrupt flags. Setting a mask bit prevents the corresponding interrupt flag from affecting the $\overline{IRQ}$ output. Clearing a mask allows the interrupt flag to affect $\overline{IRQ}$ output. Unmasking an active interrupt flag will immediately cause the $\overline{IRQ}$ output to go active, if currently inactive. Masking an active interrupt flag will cause $\overline{IRQ}$ to go inactive, if no other unmasked interrupt flags are set.

7	6	5	4	3	2	1	0
t4	t3	snr	meter	sut4	sut3	sut2	sut1

t4 General Purpose Timer 4

t3 General Purpose Timer 3

snr SNR Alarm Timer

meter Meter Timer

sut4 Startup Timer 4

sut3 Startup Timer 3

sut2 Startup Timer 2

sut1 Startup Timer 1

0x03—Interrupt Mask Register High (mask_high_reg)

Independent read/write mask bits for each of the IRQ Source Register [irq_source; 0x05] interrupt flags. Individual mask bit behavior is identical to that specified for Interrupt Mask Register Low [mask_low_reg; 0x02].

7	6	5	4	3	2	1	0
—	—	—	—	sync	high_felm	low_felm	low_snr

sync Sync Indication

high_felm Far-End Level Meter High Alarm

low_felm Far-End Level Meter High Alarm

low_snr Signal-to-Noise Ratio Low Alarm

0x04—Timer Source Register (timer_source)

Independent read/write (zero only) interrupt flags, one for each of eight internal timers. Each flag bit is set and stays set when its corresponding timer value transitions from 1 to 0. If unmasked, this event causes the $\overline{IRQ}$ output to be activated. Flags are cleared by writing them with a logical 0 value. Once a flag is cleared, a steady-state timer value of 0 does not reassert the flag. Clearing an unmasked flag causes the $\overline{IRQ}$ output to return to the inactive state, if no other unmasked interrupt flags are set.

7	6	5	4	3	2	1	0
t4	t3	snr	meter	sut4	sut3	sut2	sut1

t4 General Purpose Timer 4

t3 General Purpose Timer 3

snr SNR Alarm Timer

meter Meter Timer

sut4 Startup Timer 4

sut3 Startup Timer 3

sut2 Startup Timer 2

sut1 Startup Timer 1

0x05—IRQ Source Register (irq_source)

Independent read/write (0 only) interrupt flags, one for each of four internal sources. Each flag bit is set and stays set when its corresponding source indicates that a valid interrupt condition exists. If unmasked, this event causes the $\overline{IRQ}$ output to be activated. Writing a logical 0 to an interrupt flag whose underlying condition no longer exists causes the flag to be immediately cleared. Attempting to clear a flag whose underlying condition still exists does not immediately clear the flag, but allows it to remain set until the underlying condition expires, at which time the flag is cleared automatically. The clearing of an unmasked flag causes the $\overline{IRQ}$ output to return to an inactive state, if no other unmasked interrupt flags are set.

7	6	5	4	3	2	1	0
—	—	—	—	sync	high_felm	low_felm	low_snr

sync Sync Indication—Active when the sync detector is enabled and its accumulated equivalent comparison is greater than the threshold value stored in the Scrambler Sync Threshold Register [scr_sync_th; 0x2E].

high_felm Far-End Level Meter High Alarm—Active when the far-end level meter value is greater than the threshold stored in the Far-End High Alarm Threshold Registers [far_end_high_alarm_th_low, far_end_high_alarm_th_high; 0x30–0x31].

low_felm Far-End Level Meter Low Alarm—Active when the far-end level meter value is less than the threshold stored in the Far-End Low Alarm Threshold Registers [far_end_low_alarm_th_low, far_end_low_alarm_th_high; 0x32–0x33].

low_snr Signal-to-Noise Ratio Low Alarm—Active when the SNR Alarm meter value is greater than the threshold stored in the SNR Alarm Threshold Registers [snr_alarm_th_low, snr_alarm_th_high; 0x34–0x35].

0x06—Channel Unit Interface Modes Register (cu_interface_modes)

7	6	5	4	3	2	1	0
—	—	—	tbclk_pol	rbclk_pol	fifos_mode	interface_mode[1]	interface_mode[0]

tbclk_pol Transmit Baud Clock Polarity—Read/write control bit defines the polarity of the TBCLK input while in the parallel slave interface mode. When tbclk_pol is set, TQ[1,0] is sampled on the falling edge of TBCLK; when cleared, TQ[1,0] is sampled on the rising edge.

rbclk_pol Receive Baud Clock Polarity—Read/write control bit defines the polarity of the RBCLK input while in the parallel slave interface mode. When rbclk_pol is set, RQ[1,0] is updated on the falling edge of RBCLK; when cleared, RQ[1,0] is updated on the rising edge.

fifos_mode FIFO's Mode—Read/write control bit used to stagger the transmit and receive the FIFO's read and write pointers while in the parallel slave interface mode. A logical 1 forces the pointers to a staggered position; a logical 0 allows them to operate normally. To maximize phase-error tolerance, fifos_mode must be first set, then cleared once after QCLK-TBCLK-RBCLK frequency lock is achieved.

interface_ mode[1,0] Interface Mode—Read/write binary field specifies one of four operating modes for the channel unit interface.

Interface Mode [1:0]	Mode	Pin Functions					
		91	90	88	89	85	86
00	Parallel master—Parallel quat transfer synchronized to QCLK out.	Not used	Not used	RQ[1]	RQ[0]	TQ[1]	TQ[0]
01	Parallel slave—Parallel quat transfer synchronized to separate TBCLK and RBCLK inputs.	TBCLK	RBCLK	RQ[1]	RQ[0]	TQ[1]	TQ[0]
10	Serial, magnitude first—Serial quat transfer synchronized to BCLK out; magnitude-bit first, followed by sign bit.	Not used	Not used	RDAT	BCLK	TDAT	Not used
11	Serial, sign first—Serial quat transfer synchronized to BCLK out; sign-bit first, followed by magnitude bit.	Not used	Not used	RDAT	BCLK	TDAT	Not used

0x07—Receive Phase Select Register (receive_phase_select)

7	6	5	4	3	2	1	0
—	imp_short[2]	imp_short[1]	imp_short[0]	rphs[3]	rphs[2]	rphs[1]	rphs[0]

imp_short[2:0] Impulse Shortening Filter—Read/write binary field that determines the coefficient of the impulse shortening filter. It must be set per the software provided by Conexant.

rphs[3:0] Receive Phase Select—Read/write binary field that defines the relative phase relationship between QCLK and the sampling point of the ADC. The rising edges of QCLK correspond to the ADC sampling points when rphs equals 0000. Each binary increment of rphs represents a one-sixteenth QCLK period delay in the sampling point relative to QCLK.

0x08—Linear Echo Canceller Modes Register (linear_ec_modes)

7	6	5	4	3	2	1	0
—	—	enable_dc_tap	adapt_ coefficients	zero_coefficients	zero_output	adapt_gain[1]	adapt_gain[0]

enable_dc_tap Enable DC Tap—Read/write control bit which, when set, forces a constant + 1 value into the last data tap of the LEC. This condition enables cancellation of any residual DC offset present at the input to the LEC. When cleared, the last data tap operates normally, as the oldest transmit data sample.

adapt_coefficents Adapt Coefficients—Read/write control bit which enables coefficient adaptation when set; disables/freezes adaptation when cleared. Coefficient values are preserved when adaptation is disabled.

zero_coefficients Zero Coefficients—Read/write control bit that continuously zeros all coefficients when set; allows normal coefficient updates if enabled, when cleared. This behavior differs slightly from the similar function (zero_coefficients) of the FFE and EP filters.

zero_output Zero Output—Read/write control bit which, when set, zeros the echo replica before subtraction from the input signal. Achieves the affect of disabling or bypassing the echo cancellation function. Does not disable coefficient adaptation. When cleared, normal echo canceller operation is performed.

adapt_gain[1,0] Adaptation Gain—Read/write binary field which specifies the adaptation gain.

adapt_gain[1,0]	Normalized Gain
00	1
01	4
10	64
11	512

0x09—Nonlinear Echo Canceller Modes Register (nonlinear_ec_modes)

7	6	5	4	3	2	1	0
negate_symbol	symbol_delay[2]	symbol_delay[1]	symbol_delay[0]	adapt_ coefficients	zero_coefficients	zero_output	adapt_gain

negate_symbol Negate Symbol—Read/write control bit which, when set, inverts (2s complement) the receive signal path at the output of the nonlinear echo canceller. When cleared, the signal path is unaffected. This function is independent of all other NEC mode settings.

symbol_delay[2:0] Symbol Delay—Read/write binary field which specifies the number of symbol delays inserted in the transmit symbol input path.

adapt_coefficients Adapt Coefficients—Same function as LEC Modes Register [linear_ec_modes; 0x08].

zero_coefficients Zero Coefficients—Same function as LEC Modes Register.

zero_output Zero Output—Same function as LEC Modes Register.

adapt_gain Adaptation Gain—Read/write control bit which specifies the adaptation gain. When adapt_gain is set, the adaptation gain is eight times higher than when cleared.

0x0A—Decision Feedback Equalizer Modes Register (dfe_modes)

7	6	5	4	3	2	1	0
—	—	—	—	adapt_ coefficients	zero_coefficients	zero_output	adapt_gain

adapt_coefficents Adapt Coefficients—Read/write control bit which enables coefficient adaptation when set; disables/freezes adaptation when cleared. Coefficient values are preserved when adaptation is disabled.

zero_coefficients Zero Coefficients—Read/write control bit which continuously zeros all coefficients when set; allows normal coefficient updates, if enabled, when cleared.

zero_output Zero Output—Read/write control bit which, when set, zeros the filter output before subtraction from the FFE output. Achieves the affect of disabling or bypassing the equalization function. Does not disable coefficient adaptation. When cleared, the normal equalizer operation is performed.

adapt_gain Adaptation Gain—Read/write control bit which specifies the adaptation gain. When adapt_gain is set, the adaptation gain is eight times higher than when cleared.

0x0B—Transmitter Modes Register (transmitter_modes)

7	6	5	4	3	2	1	0
—	isolated_pulse[1]	isolated_pulse[0]	transmitter_off	htur_lfsr	data_source[2]	data_source[1]	data_source[0]

isolated_pulse[1,0] Isolated Pulse Level Select—Read/write binary field that selects one of four output pulse levels while in the isolated pulse or alternating symbol transmitter mode.

isolated_pulse[1,0]	Output Pulse Level
00	– 3
01	– 1
10	+ 3
11	+ 1

transmitter_off Transmitter Off—Read/write control bit that zeros the output of the transmitter when set; allows normal transmitter operation (as defined by data_source[2:0]) when cleared.

htur_lfsr Remote Unit (HTU-R/NT) Polynomial Select—Read/write control bit selects one of two feedback polynomials for the transmit scrambler. When set, this bit selects the remote unit transmit polynomial $(x^{-23} + x^{-18} + 1)$; when cleared, it selects the local unit (HTU-C/LT) polynomial $(x^{-23} + x^{-5} + 1)$.

data_source[2:0] Data Source—Read/write binary field that selects the data source and mode of the transmitter output. The transmitter must be enabled (transmitter_off = 0) for these modes to be active.

data_source [2:0]	Transmitter Mode
000	Isolated pulse. Level selected by isolated_pulse[1:0]. The meter timer must be enabled and in the continuous mode. The pulse repetition interval is determined by the meter timer countdown interval.
001	Four-level scrambled detector loopback. Sign and magnitude bits from the receiver detector are scrambled and looped back to the transmitter. Feedback polynomial determined by the htur_lfsr control bit.
010	Four-level unscrambled data. Transmits the four-level (2B1Q) sign and magnitude bits from the channel unit transmit interface without scrambling.
011	Four-level scrambled 1s. Transmits a scrambled, constant high-logic level as a four-level (2B1Q) signal. Feedback polynomial determined by the htur_lfsr control bit.
100	Alternating symbol mode. Outputs symbols of alternating polarity. Level is selected by isolated_pulse[1:0]. The meter timer must be enabled and in continuous mode. The half period of the output signal is defined by the meter timer countdown interval.
101	Four-level scrambled data. Scrambles and transmits the four-level (2B1Q) sign and magnitude bits from the channel unit transmit interface. Feedback polynomial determined by the htur_lfsr control bit.
110	Two-level unscrambled data. Constantly forces the magnitude bit from the channel unit transmit interface to a logical 0 and transmits the resulting two-level signal (as determined by the sign bit) without scrambling. Valid output levels limited to + 3, – 3.
111	Two-level scrambled 1s. Transmits a scrambled, constant high-logic level as a two-level signal. The feedback polynomial is determined by the htur_lfsr control bit. The scrambler is run at the symbol rate (half-bit rate) to produce the sign bit of the transmitted signal while the magnitude bit is sourced with a constant logical 0. Valid output levels are limited to + 3, – 3.

0x0C—Timer Restart Register (timer_restart)

Independent read/write restart bits, one for each of the eight internal timers. Setting an individual bit causes the associated timer to be reloaded with the contents of its interval register. For the four symbol-rate timers (meter, snr, t3, t4), reloading occurs within 1 symbol period. For the four start-up timers (sut1–4), reloading occurs within 1024 symbol periods. Once the timer is reloaded, the restart bit is automatically cleared. If a restart bit is set and then cleared (by writing a logical 0) before the reload actually takes place, no timer reload occurs. Once reloaded, if enabled in the Timer Enable Register [timer_enable; 0x0D], the timer begins counting down toward zero; otherwise, it holds at the interval register value.

7	6	5	4	3	2	1	0
t4	t3	snr	meter	sut4	sut3	sut2	sut1

t4 General Purpose Timer 4

t3 General Purpose Timer 3

snr SNR Alarm Timer

meter Meter Timer

sut4 Startup Timer 4

sut3 Startup Timer 3

sut2 Startup Timer 2

sut1 Startup Timer 1

0x0D—Timer Enable Register (timer_enable)

Independent read/write enable bits, one for each of the eight internal timers. When any individual bit is set, the corresponding timer is enabled for counting down from its current value toward 0. For the four symbol-rate timers (meter, snr, t3, t4), counting begins within 1 symbol period. For the four start-up timers (sut1-4), counting begins within 1024 symbol periods. When an enable bit is cleared, the timer is disabled from counting and holds its current value. If an enable bit is set and then cleared before a count actually takes place, no timer countdown occurs.

7	6	5	4	3	2	1	0
t4	t3	snr	meter	sut4	sut3	sut2	sut1

t4 General Purpose Timer 4

t3 General Purpose Timer 3

snr SNR Alarm Timer

meter Meter Timer

sut4 Startup Timer 4

sut3 Startup Timer 3

sut2 Startup Timer 2

sut1 Startup Timer 1

0x0E—Timer Continuous Mode Register (timer_continuous)

Independent read/write mode bits, one for each of the eight internal timers. When any individual bit is set, the corresponding timer is placed in the continuous count mode. While in this mode, after reaching the 0 count, an enabled timer will reload the contents of its interval register and continue counting. When a mode bit is cleared, the timer is taken out of the continuous mode. While in this configuration, after reaching the zero count, an enabled timer will simply stop counting and remain at 0.

7	6	5	4	3	2	1	0
t4	t3	snr	meter	sut4	sut3	sut2	sut1

For a description of bit-fields, refer to the description given above for register *0x0D—Timer Enable Register (timer_enable)*.

0x0F—Miscellaneous/Test Register (misc_test)

A 1-byte read/write register that is automatically initialized to 0x00 upon $\overline{\text{RST}}$ assertion and initial power application.

7	6	5	4	3	2	1	0
res[6]	res[5]	reg_clk_en	res[4]	res[3]	res[2]	res[1]	async_mode

res[6:1] Reserved Bits—Read/write binary field that is automatically initialized to 0x00 upon $\overline{\text{RST}}$ assertion and initial power application.

reg_clk_en Regenerator Clock Enable—When set, it bypasses the frequency synthesizer and timing recovery. In this mode, the symbol rate equals MCLK ÷ 16. Normally this bit is reset and should be set only for the transceiver configured as REG–C in a regenerator configuration. Refer to Section 1.3, *Regenerator Configuration*.

async_mode Asynchronous Mode—Read/write control bit that selects asynchronous MCI timing mode, when set. When reset it selects synchronous mode MCI timing. Refer to Table 5-13, *Microcomputer Interface Timing Requirements*, and Table 5-14, *Microcomputer Interface Switching Characteristics*, for MCI timing requirements and switching characteristics.

0x10, 0x11—Startup Timer 1 Interval Register (sut1_low, sut1_high)

A 2-byte read/write register that stores the countdown interval for Startup Timer 1 in unsigned binary format. Each increment represents 1024 symbol periods. The contents of this register are automatically loaded into its associated timer after the timer's timer_restart bit is set, or after it counts down to zero while in the continuous mode.

0x12, 0x13—Startup Timer 2 Interval Register (sut2_low, sut2_high)

A 2-byte read/write register that stores the countdown interval for Startup Timer 2 in unsigned binary format. Each increment represents 1024 symbol periods. The contents of this register are automatically loaded into its associated timer after the timer's timer_restart bit is set, or after it counts down to zero while in the continuous mode.

0x14, 0x15—Startup Timer 3 Interval Register (sut3_low, sut3_high)

A 2-byte read/write register that stores the countdown interval for Startup Timer 3 in unsigned binary format. Each increment represents 1024 symbol periods. The contents of this register are automatically loaded into its associated timer after the timer_restart bit is set, or after the timer counts down to zero while in the continuous mode.

0x16, 0x17—Startup Timer 4 Interval Register (sut4_low, sut4_high)

A 2-byte read/write register that stores the countdown interval for Startup Timer 4 in unsigned binary format. Each increment represents 1024 symbol periods. The contents of this register are automatically loaded into its associated timer after the timer's timer_restart bit is set, or after it counts down to zero while in the continuous mode.

0x18, 0x19—Meter Timer Interval Register (meter_low, meter_high)

A 2-byte read/write register that stores the countdown interval for the Meter Timer in unsigned binary format. Each increment represents one symbol period. The contents of this register are automatically loaded into its associated timer after the timer's timer_restart bit is set, or after it counts down to zero while in the continuous mode.

0x1A, 0x1B—SNR Alarm Timer Interval Register (snr_timer_low, snr_timer_high)

A 2-byte read/write register that stores the countdown interval for the SNR Alarm Timer in unsigned binary format. Each increment represents one symbol period. The contents of this register are automatically loaded into its associated timer after the timer's timer_restart bit is set, or after it counts down to zero while in the continuous mode.

0x1C, 0x1D—General Purpose Timer 3 Interval Register (t3_low, t3_high)

A 2-byte read/write register that stores the countdown interval for General Purpose Timer 3 in unsigned binary format. Each increment represents one symbol period. The contents of this register are automatically loaded into its associated timer after the timer's timer_restart bit is set, or after it counts down to zero while in the continuous mode.

0x1E, 0x1F—General Purpose Timer 4 Interval Register (t4_low, t4_high)

A 2-byte read/write register that stores the countdown interval for General Purpose Timer 4 in unsigned binary format. Each increment represents one symbol period. The contents of this register are automatically loaded into its associated timer after the timer's timer_restart bit is set, or after it counts down to zero while in the continuous mode.

0x20—Clock Frequency Select Register (clock_freq_select)

7	6	5	4	3	2	1	0
clk_freq[7]	clk_freq[6]	clk_freq[5]	clk_freq[4]	clk_freq[3]	clk_freq[2]	clk_freq[1]	clk_freq[0]

clk_freq[7:0] Read/write binary field, which along with clk_freq[9,8] of the PLL Modes Register (0x22), specifies the data rate used by the clock synthesizer to generate the appropriate internal clock.

clk_freq = 18 to 290
data rate = clk_freq × 8 kbps (144 kbps to 2320 kbps)

The power-on default is clk_freq = 0 which selects the internal clock corresponding to 1280 kbps.

0x21—ADC Control Register (adc_control)

7	6	5	4	3	2	1	0
cont_time[1]	cont_time[0]	loop_back[1]	loop_back[0]	switch_cap_pole	gain[2]	gain[1]	gain[0]

cont_time[1,0] Continuous Time Control—Read/write binary field that controls the cut-off frequency of the analog RC reconstruction filter, according to the data rates.

cont_time[1,0]	Data Rate Range
00	800 to 1200 kbps
01	Less than 800 kbps
10	Above 1200 kbps
11	Reserved

The “00” setting of the continuous_time control bits enables an output pulse shape that conforms to the ETSI HDSL specifications at 1168 kbps.

The “01” setting enables an output pulse shape that conforms to the ANSI and ETSI HDSL specifications at 784 kbps.

The “10” setting enables an output pulse shape that conforms to the ETSI HDSL specifications at 2320 kbps.

loop_back[1,0] Loopback Control—Read/write binary field that specifies if loopback is enabled, and the type of loopback that is enabled. During transmitting loopback, the differential receiver inputs (RXP, RXN) are disabled. The loopback path is intended to go from the transmitter outputs (TXP, TXN) through the external hybrid circuit and back into the differential receiver balance inputs (RXBP, RXBN). During silent loopback, the transmitter is turned off. The output of the pulse-shaping filter in the transmit section is internally connected to the input of the ADC in the receive section.

loop_back[1,0]	Function
00	Normal Operation (Loopback Disabled)
01	Hybrid Inputs Disabled (RXBP, RXBN)
10	Transmitting Loopback
11	Silent Loopback

switch_cap_pole Switch Cap Pole Control—Read/write control bit, specifies the pulse shaping filter characteristics. When switch_cap_pole is set, it enables output pulse shape conforming to ETSI specifications for 2320 kbps operation. When reset, it enables output pulse shape for other data rates.

gain[2:0] Gain Control—Read/write binary field that specifies the gain of the VGA.

gain[2:0]	VGA Gain
000	0 dB
001	3 dB
010	6 dB
011	9 dB
100	12 dB
101	15 dB
110	15 dB
111	15 dB

0x22—PLL Modes Register (pll_modes)

7	6	5	4	3	2	1	0
clk_freq[9]	clk_freq[8]	—	phase_detector_ gain[1]	phase_detector_ gain[0]	freeze_pll	pll_gain[1]	pll_gain[0]

clk_freq[9,8] Clock Frequency Select—See description for *0x20—Clock Frequency Select Register (clock_freq_select)*.

phase_detector_ gain[1,0] Phase Detector Gain—Read/write binary field that specifies one of three gain settings for the timing-recovery phase detector function.

phase_detector_gain[1,0]	Normalized Gain
00	1
01	2
10	4
11	Reserved

freeze_pll Freeze PLL—Read/write control bit. When set, this bit zeros the proportional term of the loop compensation filter and disables accumulator updates, causing the PLL to hold its current frequency. When this bit is cleared, proportional term effects and accumulator updates are enabled, allowing the PLL to track the phase of the incoming data.

pll_gain[1,0] PLL Gain—Read/write binary field that specifies the gain (proportional and integral coefficients) of the loop compensation filter.

pll_gain[1:0]	Normalized Proportional Coefficients	Normalized Integral Coefficients
00	1	1
01	4	32
10	16	256
11	64	4096

0x23—Test Register (test_reg23)

A 3-byte read/write register used for device testing by Conexant. This register is automatically initialized to 0x000000 upon $\overline{\text{RST}}$ assertion and initial power application. This register must be initialized according to the software provided by Conexant.

0x24, 0x25—Timing Recovery PLL Phase Offset Register (pll_phase_offset_low, pll_phase_offset_high)

A 2-byte read/write register interpreted as a 16-bit, 2s-complement number. The value of this register is subtracted from the output of the timing-recovery phase detector after the phase-detector meter, but before the loop compensation filter.

0x26, 0x27—Receiver DC Offset Register (dc_offset_low, dc_offset_high)

A 2-byte read/write register interpreted as a 16-bit, 2s-complement number. The value of this register is subtracted from the receiver signal path at the output of the ADC block, ahead of the DC level and signal level meters.

0x28—Transmitter Calibration Register (tx_calibrate)

7	6	5	4	3	2	1	0
—	—	tx_calibrate[3]	tx_calibrate[2]	tx_calibrate[1]	tx_calibrate[0]	—	—

tx_calibrate[3:0] Transmit Calibrate—4-bit, 2s-complement, read-only field containing the nominal setting for the transmitter gain. The value of the Transmit Calibration Register is set during manufacturing testing by Conexant, and corresponds to the value required to operate the RS8973 at a nominal 13.5 dBm transmit power, assuming the recommended transformer coupling/hybrid circuit is used. Users can override this calibration by writing their own value into the Transmitter Gain Register [tx_gain; 0x29].

0x29—Transmitter Gain Register (tx_gain)

7	6	5	4	3	2	1	0
—	—	tx_gain[3]	tx_gain[2]	tx_gain[1]	tx_gain[0]	—	—

tx_gain[3:0] Transmit Gain—A 4-bit, 2s-complement, read/write field controlling the transmitter gain. Upon initialization, the value in the Transmitter Calibration Register [tx_calibrate; 0x28] can be written into this register by software, to set the transmitter gain to the nominal value. Alternatively, the user can set it to another desired value. The transmitter gain settings are relative to the setting that provides a nominal output power of 13.5 dBm.

tx_gain[3:0]	Relative Transmitter Gain (dB)
1000	–1.60
1001	–1.36
1010	–1.13
1011	–0.91
1100	–0.69
1101	–0.48
1110	–0.27
1111	–0.07
0000	0.13
0001	0.32
0010	0.51
0011	0.70
0100	0.88
0101	1.05
0110	1.23
0111	1.40

0x2A, 0x2B—Noise-Level Histogram Threshold Register (noise_histogram_th_low, noise_histogram_th_high)

A 2-byte read/write register interpreted as a 16-bit, 2s-complement number. The range of meaningful values is limited to positive integers between 0x0000 and 0x7FFF. The value of this register is compared to the absolute value of the slicer error signal produced by the detector. A count of error samples that exceeds this threshold (greater than) is accumulated in the noise-level histogram meter.

0x2C, 0x2D—Error Predictor Pause Threshold Register (ep_pause_th_low, ep_pause_th_high)

A 2-byte read/write register interpreted as a 16-bit, 2s-complement number. The range of meaningful values is limited to positive integers between 0x0000 and 0x7FFF. The value of this register is compared to the absolute value of the slicer error signal produced by the detector. The result of this comparison (slicer error greater than this threshold) is used to initiate a pause condition by zeroing the output of the error predictor correction signal before subtraction from the receive signal path. Error predictor coefficient updates are not affected. The pause condition lasts for a fixed 5-symbol period from the time the threshold was last exceeded.

0x2E—Scrambler Synchronization Threshold Register (scr_sync_th)

A 7-bit read/write register representing an unsigned binary number. The contents of this register are used to test for scrambler synchronization during the automatic-scrambler synchronization mode of the symbol detector. The test passes when the count of equivalent scrambler and detector output bits is greater than the value of this register. When the auto-scrambler sync mode is not enabled, the contents of this register are not used.

7	6	5	4	3	2	1	0
—	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x30, 0x31—Far-End High Alarm Threshold Register (far_end_high_alarm_th_low, far_end_high_alarm_th_high)

A 2-byte read/write register interpreted as a 16-bit, 2s-complement number. The range of meaningful values is limited to positive integers between 0x0000 and 0x7FFF. The value of this register is compared to the value of the far-end level meter. If the meter reading is greater than this threshold, the high_felm interrupt flag is set in the IRQ Source Register [irq_source; 0x05].

0x32, 0x33—Far-End Low Alarm Threshold Register (far_end_low_alarm_th_low, far_end_low_alarm_th_high)

A 2-byte read/write register interpreted as a 16-bit, 2s-complement number. The range of meaningful values is limited to positive integers between 0x0000 and 0x7FFF. The value of this register is compared to the value of the far-end level meter. If the meter reading is less than this threshold, the low_felm interrupt flag is set in the IRQ Source Register [irq_source; 0x05].

0x34, 0x35—SNR Alarm Threshold Register (snr_alarm_th_low, snr_alarm_th_high)

A 2-byte read/write register interpreted as a 16-bit, 2s-complement number. The range of meaningful values is limited to positive integers between 0x0000 and 0x7FFF. The value of this register is compared to the value of the SNR alarm meter. If the meter reading is greater than this threshold, the low_snr interrupt flag is set in the IRQ Source Register [irq_source; 0x05].

0x36, 0x37—Cursor Level Register (cursor_level_low, cursor_level_high)

A 2-byte read/write register interpreted as a 16-bit, 2s-complement number. The range of meaningful values is limited to positive integers between 0x0000 and 0x2AAA (one-third of the maximum positive value). The value of this register represents the expected level of a noise-free + 1 receive symbol at the slicer input. It is multiplied by 2 to produce the positive and negative slicing levels, in addition to 0, used by the symbol detector in four-level slicing mode. This value is also used to scale the detector output when computing the equalizer error and slicer error signals. The detected symbol (– 3, – 1, + 1, + 3) is multiplied by the value of this register to produce the scaled output.

0x38, 0x39—DAGC Target Register (dagc_target_low, dagc_target_high)

A 2-byte read/write register interpreted as a 16-bit, 2s-complement number. The range of meaningful values is limited to positive integers between 0x0000 and 0x7FFF. The value of this register is subtracted from the absolute value of the receive signal at the output of the DAGC function. The difference is used as the error input to the DAGC while in the self-adaptation mode. In the DAGC's equalizer-error adaptation mode, the contents of this register are not used.

0x3A—Symbol Detector Modes Register (detector_modes)

7	6	5	4	3	2	1	0
enable_peak_ detector	output_mux_ control[1]	output_mux_ control[0]	scr_out_to_dfe	two_level	lfsr_lock	htur_lfsr	descr_on

enable_peak_ detector Enable Peak Detector—Read/write control bit that enables the peak detection function when set; disables the function when cleared. When enabled, the peak detector output overrides the slicer output if the peak detection criteria are met. If the criteria are not met, or if the function is disabled, the slicer output is used and peak detector output is ignored.

output_mux_ control[1,0] Output Multiplexer Control—Read/write binary field that selects the source of the detector output connected to the channel unit receive interface.

output_mux_control[1,0]	Detector Output to CU Receive Interface
00	Same as scr_out_to_dfe selection
01	Transmitter loopback output from CU transmit interface
10	Scrambler/descrambler output
11	Reserved

scr_out_to_dfe Scrambler Output to DFE—Read/write control bit that selects the source of the detector output connected to the DFE and timing recovery module inputs and the transmitter's detector loopback input. When set, this bit selects the scrambler/descrambler function; when cleared, it selects the slicer/peak detector output.

two_level Two-Level Mode—Read/write control bit that selects two-level mode when set, four-level mode when cleared. Affects the slicer and the scrambler/descrambler function. In two-level mode, the slicer uses a single threshold set at zero to recover sign bits only; all magnitude information is lost. Scrambler/descrambler updates are slowed to the symbol rate (half the normal bit rate) to process only sign information as well; all magnitude output bits are sourced with a constant logic zero value, producing two-level symbols constrained to +3 and –3 values.

In four-level mode, the slicer uses two thresholds derived from the Cursor Level Register [cursor_level_low, cursor_level_high; 0x36–0x37], as well as the zero threshold, to recover both sign and magnitude information. The scrambler/descrambler is updated at the full bit rate to process both sign and magnitude bits as well.

lfsr_lock LFSR Lock—Read/write control bit that enables the auto-scrambler synchronization mode (lfsr_lock) in the detector when set and disables this mode when cleared. Affects the behavior of the scrambler/descrambler function, overriding the descr_on setting. When enabled, the scrambler/descrambler is forced into the descrambler mode for 23 cycles. It is then switched to the scrambled-1s mode for 128 cycles. While in this mode, the outputs of the scrambler and the slicer/peak detector are compared against one another. The number of equivalent bits (equal comparisons) is accumulated and compared to the value of the Scrambler Synchronization Threshold Register [scr_sync_th; 0x2E].

At any time during the 128 cycles, if the count exceeds the threshold (greater than), the sync interrupt flag is set in the IRQ source register [irq_source; 0x05] and the process terminates with the scrambler/descrambler left in the scrambled-1s mode. (The sync interrupt flag cannot be cleared while lfsr_lock remains high.) After 128 cycles, if the threshold is not exceeded, the accumulator is cleared, the scrambler/descrambler re-enters the descrambler mode for another 23 cycles, and the process repeats until either sync is achieved or this mode is disabled. Once disabled, the sync interrupt flag can be cleared (if active) and the scrambler/descrambler returns to the mode specified by descr_on.

htur_lfsr Remote Unit (HTU-R/NT) Polynomial Select—Read/write control bit that selects one of two feedback polynomials for the scrambler/descrambler. When set, this bit selects the remote unit (HTU-R/NT) receive polynomial ($x^{-23} + x^{-5} + 1$); when cleared, it selects the local unit (HTU-C/LT) polynomial ($x^{-23} + x^{-18} + 1$).

descr_on Descrambler/Scrambler Select—Read/write control bit that configures the scrambler/descrambler function as a descrambler when set, and as a scrambler when cleared. As a scrambler, this bit enables the scrambler/descrambler to generate a scrambled-all-1s sequence (constant high logic-level input); all incoming data is ignored. In the auto-scrambler synchronization mode (lfsr_lock = 1), this selection is overwritten though the value of the control bit is unaffected.

0x3B—Peak Detector Delay Register (peak_detector_delay)

A 4-bit read/write register interpreted as an unsigned binary number. Specifies a number of additional symbol delays inserted in the peak detector input path of the symbol detector. Must be set to a value that equalizes the total path delay in each of the peak detector and slicer input paths according to the following formula: peak detector delay register value = DAGC delays + FFE delays – fixed peak detector input delays. The DAGC and FFE delays are not fixed, but result from the microprogrammed implementation of these functions. The value should be set according to software supplied by Conexant.

7	6	5	4	3	2	1	0
—	—	—	—	D[3]	D[2]	D[1]	D[0]

0x3C—Digital AGC Modes Register (dagc_modes)

7	6	5	4	3	2	1	0
—	—	—	—	—	eq_error_ adaptation	adapt_coefficients	adapt_gain

eq_error_ adaptation Equalizer Error Adaptation—Read/write control bit that selects between the equalizer-error adaptation mode when set, and the self-adaptation mode when cleared. Equalizer error adaptation uses the equalizer error signal produced by the slicer as the DAGC error input signal. In self-adaptation, the value of the DAGC Target Register [dagc_target_low, dagc_target_high; 0x38–0x39] is subtracted from the absolute value of the receive signal at the output of the DAGC, and this difference is used as the error input signal.

adapt_coefficients Adapt Coefficients—Read/write control bit that enables coefficient adaptation when set; disables/freezes adaptation when cleared. Coefficient values are preserved when adaptation is disabled.

adapt_gain Adaptation Gain—Read/write control bit that specifies the adaptation gain. When this bit is set, the adaptation gain is eight times higher than when cleared.

0x3D—Feed Forward Equalizer Modes Register (ffe_modes)

7	6	5	4	3	2	1	0
—	—	—	—	adapt_last_coeff	zero_coefficents	adapt_ coefficients	adapt_gain

adapt_last_coeff Adapt Last Coefficient—Read/write control bit that enables adaptation of the last (oldest) coefficient only when set; allows all coefficient adaptation when cleared. Overall coefficient adaptation must be enabled (adapt_coefficients = 1) for this behavior to occur. If coefficient adaptation is disabled (adapt_coefficients = 0), the value of this control bit is not used.

zero_coefficients Zero Coefficients—Read/write control bit that, with coefficient adaptation enabled (adapt_coefficients = 1), continuously zeros all coefficients when set; allows normal coefficient updates when cleared. If coefficient adaptation is disabled (adapt_coefficients = 0), this control bit has no affect. This behavior differs slightly from the similar function (zero_coefficients) of the LEC, NEC, and DFE filters. Whenever this bit is set, it must be accompanied by adapt_coefficients (set) for a 2-symbol time period.

adapt_coefficents Adapt Coefficients—Read/write control bit that enables coefficient adaptation when set; disables/freezes adaptation when cleared. Coefficient values are preserved when adaptation is disabled. This overall coefficient adaptation must be enabled for adapt_last_coeff to have an affect.

adapt_gain Adaptation Gain—Read/write control bit that specifies the adaptation gain. When set, the adaptation gain is four times higher than when cleared.

0x3E—Error Predictor Modes Register (ep_modes)

7	6	5	4	3	2	1	0
—	—	—	—	zero_output	zero_coefficients	adapt_ coefficients	adapt_gain

zero_output Zero Output—Read/write control bit that, when set, zeros the error predictor correction signal before subtraction at the slicer. Achieves the affect of disabling, or bypassing, the error predictor function. Does not disable coefficient adaptation. When cleared, normal error predictor operation is performed.

zero_coefficients Zero Coefficients—Read/write control bit that, with coefficient adaptation enabled (adapt_coefficients = 1), continuously zeros all coefficients when set; allows normal coefficient updates when cleared. If coefficient adaptation is disabled (adapt_coefficients = 0), this control bit has no affect. This behavior differs slightly from the similar function (zero_coefficients) of the LEC, NEC, and DFE filters. Whenever this bit is set, it must be accompanied by adapt_coefficients (set) for a 2-symbol time period.

adapt_coefficents Adapt Coefficients—Read/write control bit that enables coefficient adaptation when set and disables/freezes adaptation when cleared. Coefficient values are preserved when adaptation is disabled.

adapt_gain Adaptation Gain—Read/write control bit that specifies the adaptation gain. When this bit is set, the adaptation gain is four times higher than when cleared.

0x40, 0x41—Phase Detector Meter Register (pdm_low, pdm_high)

A 2-byte read-only register containing the 16 MSBs of the 26-bit, 2s-complement phase detector meter accumulator. This meter sums the output of the timing recovery module's phase detector over each Meter Timer countdown interval, before being offset by the Phase Offset Register [pll_phase_offset_low, pll_phase_offset_high; 0x24, 0x25]. Automatically loaded at the end of each interval, the meter register must be read low byte first, followed by high byte, unseparated by any other meter access (addresses 0x40 to 0x5F).

7	6	5	4	3	2	1	0
D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]
D[25]	D[24]	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]

0x42—Overflow Meter Register (overflow_meter)

A single-byte read-only register containing all 8 bits of the unsigned overflow meter accumulator. This meter counts the number of ADC overflow conditions which occur during each meter timer countdown interval, limited to a maximum count of 255 (0xFF). The meter register is automatically loaded at the end of each countdown interval.

7	6	5	4	3	2	1	0
D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x44, 0x45—DC Level Meter Register (dc_meter_low, dc_meter_high)

A 2-byte read-only register containing the 16 MSBs of the 32-bit, 2s-complement DC-level meter accumulator. This meter sums the value of the receive signal input path—after DC offset correction but before echo cancellation—over each Meter Timer countdown interval. Automatically loaded at the end of each interval, the meter register must be read low byte first, followed by high byte, unseparated by any other meter access (addresses 0x40 to 0x5F).

7	6	5	4	3	2	1	0
D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]
D[31]	D[30]	D[29]	D[28]	D[27]	D[26]	D[25]	D[24]

0x46, 0x47—Signal Level Meter Register (slm_low, slm_high)

A 2-byte read-only register containing 16 MSBs of the 32-bit unsigned signal-level meter accumulator. This meter sums the absolute value of the receive signal input path—after DC offset correction but before echo cancellation (same point as the DC level meter)—over each Meter Timer countdown interval. Automatically loaded at the end of each interval, the meter register must be read low byte first, followed by high byte, unseparated by any other meter access (addresses 0x40 to 0x5F).

7	6	5	4	3	2	1	0
D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]
D[31]	D[30]	D[29]	D[28]	D[27]	D[26]	D[25]	D[24]

0x48, 0x49—Far-End Level Meter Register (felm_low, felm_high)

A 2-byte read-only register containing 16 MSBs of the 32-bit unsigned far-end level meter accumulator. This meter sums the absolute value of the receive signal path—after echo cancellation but before the DAGC function—over each Meter Timer countdown interval. Automatically loaded at the end of each interval, this meter register must be read low byte first, followed by high byte, unseparated by any other meter access (addresses 0x40 to 0x5F).

7	6	5	4	3	2	1	0
D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]
D[31]	D[30]	D[29]	D[28]	D[27]	D[26]	D[25]	D[24]

0x4A, 0x4B—Noise Level Histogram Meter Register (noise_histogram_low, noise_histogram_high)

A 2-byte read-only register containing all 16 bits of the unsigned noise-level histogram meter accumulator. This meter counts the number of high-noise-level conditions which occur during each Meter Timer countdown interval. A high-noise-level condition is defined as the absolute value of the slicer error signal exceeding (greater than) the threshold specified in the Noise-level Histogram Threshold Register [0x2A, 2B]. Automatically loaded at the end of each countdown interval, this meter register must be read low byte first, followed by high byte, unseparated by any other meter access (addresses 0x40 to 0x5F).

7	6	5	4	3	2	1	0
D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]

0x4C, 0x4D—Bit Error Rate Meter Register (ber_meter_low, ber_meter_high)

A 2-byte read-only register containing all 16 bits of the unsigned BER meter accumulator. This meter counts the number of error-free bits recovered by the detector during each Meter Timer countdown interval. An error-free bit is defined as a match (equal comparison) of the detector's slicer/peak detector output and its scrambler/descrambler output, when operating as a scrambler. When the scrambler/descrambler is operated as a descrambler, the meter simply counts the number of logical 1s produced by the descrambler. The meter register is automatically loaded at the end of each countdown interval, and must be read low byte first, followed by high byte, unseparated by any other meter access (addresses 0x40 to 0x5F).

7	6	5	4	3	2	1	0
D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]

0x4E—Symbol Histogram Meter Register (symbol_histogram)

A single-byte read-only register containing 8 MSBs of the 16-bit unsigned symbol histogram meter accumulator. This meter counts the number of + 1 or – 1 symbols detected during each Meter Timer countdown interval. No increment occurs when a + 3 or – 3 symbol is detected. The meter register is automatically loaded at the end of each countdown interval.

7	6	5	4	3	2	1	0
D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x50, 0x51—Noise Level Meter Register (nlm_low, nlm_high)

A 2-byte read-only register containing 16 MSBs of the 32-bit unsigned noise-level meter accumulator. This meter sums the absolute value of the detector's slicer-error signal over each Meter Timer countdown interval. Automatically loaded at the end of each interval, the meter register must be read the low byte first, followed by high byte, unseparated by any other meter access (addresses 0x40 to 0x5F).

7	6	5	4	3	2	1	0
D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]
D[31]	D[30]	D[29]	D[28]	D[27]	D[26]	D[25]	D[24]

0x5E, 0x5F— PLL Frequency Register (pll_frequency_low, pll_frequency_high)

A 2-byte read/write register comprising 16 MSBs of the 31-bit, 2s-complement timing recovery loop compensation filter accumulator. Treated much like a meter register, the frequency register must be read low byte first, followed by high byte, unseparated by any other meter access (addresses 0x40 to 0x5F). Writes must occur in the same order, with the low byte written first, followed by the high byte. Write accesses can be separated by any number of other read or write accesses.

7	6	5	4	3	2	1	0
D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]	D[15]
D[30]	D[29]	D[28]	D[27]	D[26]	D[25]	D[24]	D[23]

0x70—LEC Read Tap Select Register (linear_ec_tap_select_read)

A 7-bit read/write register representing an unsigned binary address defined over a range of 0 to 119 decimal. When written, it causes the selected 32-bit coefficient of the LEC to be subsequently loaded into the Access Data Register [access_data_byte[3:0]; 0x7C–0x7F] within 2 symbol periods. Does not affect the value of the coefficient. No other data access should occur between the time the Read Tap Select Register is written and the time the Access Data Register is read, or the data may be corrupted.

7	6	5	4	3	2	1	0
—	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x71—LEC Write Tap Select Register (linear_ec_tap_select_write)

A 7-bit read/write register representing an unsigned binary address defined over a range of 0 to 119 decimal. When written, it causes all 32 bits of the Access Data Register [access_data_byte[3:0]; 0x7C–0x7F] to be subsequently written to the selected LEC coefficient within 2 symbol periods. Does not affect the value of the access data register.

7	6	5	4	3	2	1	0
—	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x72—NEC Read Tap Select Register (nonlinear_ec_tap_select_read)

A 6-bit read/write register representing an unsigned binary address defined over a range of 0 to 63 decimal. When written, this register causes the selected 14-bit coefficient of the NEC to be subsequently loaded into the lowest-order bits of the Access Data Register [access_data_byte[3:0]; 0x7C–0x7F] within 2 symbol periods. Does not affect the value of the coefficient. No other data access should occur between the time the Read Tap Select Register is written and the time the Access Data Register is read, or the data may be corrupted.

7	6	5	4	3	2	1	0
—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x73—NEC Write Tap Select Register (nonlinear_ec_tap_select_write)

A 6-bit read/write register representing an unsigned binary address defined over a range of 0 to 63 decimal. When written, this register causes the lowest-order 14 bits of the Access Data Register [access_data_byte[3:0]; 0x7C–0x7F] to be subsequently written to the selected NEC coefficient within 2 symbol periods. Does not affect the value of the access data register.

7	6	5	4	3	2	1	0
—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x74—DFE Read Tap Select Register (dfe_tap_select_read)

A 7-bit read/write register representing an unsigned binary address defined over a range of 0 to 115 decimal. When written, this register causes the selected 16-bit coefficient of the DFE to be subsequently loaded into the lowest-order bits of the Access Data Register [access_data_byte[3:0]; 0x7C–0x7F] within 2 symbol periods. Does not affect the value of the coefficient. No other data access should occur between the time the Read Tap Select Register is written and the time the Access Data Register is read, or the data may be corrupted.

7	6	5	4	3	2	1	0
—	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x75—DFE Write Tap Select Register (dfe_tap_select_write)

A 7-bit read/write register representing an unsigned binary address defined over a range of 0 to 115 decimal. When written, this register causes the lowest-order 16 bits of the Access Data Register [access_data_byte[3:0]; 0x7C–0x7F] to be subsequently written to the selected DFE coefficient within 2 symbol periods. Does not affect the value of the access data register.

7	6	5	4	3	2	1	0
—	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x76—Scratch Pad Read Tap Select (sp_tap_select_read)

A 6-bit read/write register representing an unsigned binary address defined over a range of 0 to 63 decimal. When written, this register causes the selected 8-bit scratch pad memory location to be subsequently loaded into the lowest-order bits of the Access Data Register [access_data_byte[3:0]; 0x7C–0x7F] within 2 symbol periods. Does not affect the value of the memory. No other data access should occur between the time the Read Tap Select Register is written and the time the Access Data Register is read, or the data may be corrupted.

7	6	5	4	3	2	1	0
—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x77—Scratch Pad Write Tap Select (sp_tap_select_write)

A 6-bit read/write register representing an unsigned binary address defined over a range of 0 to 63 decimal. When written, this register causes the lowest-order 8 bits of the Access Data Register [access_data_byte[3:0]; 0x7C–0x7F] to be subsequently written to the selected scratch pad memory location within 2 symbol periods. Does not affect the value of the access data register.

7	6	5	4	3	2	1	0
—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x78—Equalizer Read Select Register (eq_add_read)

A 6-bit read/write register representing an unsigned binary address defined over a range of 0 to 47 decimal. When written, this register causes the selected 16-bit location of the equalizer register file to be subsequently loaded into the lowest-order bits of the Access Data Register [access_data_byte[3:0]; 0x7C–0x7F] within 2 symbol periods. Does not affect the value of the register file location. An address map of the shared register file, as defined by the factory-delivered microcode, is displayed in Table 3-2. No other data access should occur between the time the Read Tap Select Register is written and the time the Access Data Register is read, or the data may be corrupted.

7	6	5	4	3	2	1	0
—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

Table 3-2. Address Map of Shared Register Fill

D[5:0]		Stored Parameter
Decimal	Binary	
0–7	00 0000–00 0111	FFE Coefficients 0–7
8–15	00 1000–00 1111	FFE Data Taps 0–7
16–20	01 0000–01 0100	EP Coefficients 0–4
21–25	01 0101–01 1001	EP Data Taps 0–4
26	01 1010	DAGC Gain—Least-Significant Word
27	01 1011	DAGC Gain—Most-Significant Word
28	01 1100	DAGC Output
29	01 1101	FFE Output
30	01 1110	DAGC Input
31	01 1111	FFE Output, Delayed 1 Symbol Period
32	10 0000	DAGC Error Signal
33	10 0001	Equalizer Error Signal
34	10 0010	Slicer Error Signal
35–47	10 0011–10 1111	Reserved

0x79—Equalizer Write Select Register (eq_add_write)

A 6-bit read/write register representing an unsigned binary address defined over a range of 0 to 47 decimal. When written, this register causes the lowest-order 16 bits of the Access Data Register [access_data_byte[3:0]; 0x7C–0x7F] to be subsequently written to the selected equalizer register file location within 2 symbol periods. Does not affect the value of the access data register. An address map of the shared register file, as defined by the factory-delivered microcode, is displayed in Table 3-2, *Address Map of Shared Register Fill*.

7	6	5	4	3	2	1	0
—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x7A—Equalizer Microcode Read Select Register (eq_microcode_add_read)

A 6-bit read/write register representing an unsigned binary address defined over a range of 0 to 63 decimal. When written, this register causes the selected 32-bit location of the equalizer microprogram store to be subsequently loaded into the Access Data Register [access_data_byte[3:0]; 0x7C–0x7F] within 2 symbol periods. Does not affect the value of the microprogram store location. No other data access should occur between the time the Read Tap Select Register is written and the time the Access Data Register is read, or the data may be corrupted.

7	6	5	4	3	2	1	0
—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x7B—Equalizer Microcode Write Select Register (eq_microcode_add_write)

A 6-bit read/write register representing an unsigned binary address defined over a range of 0 to 63 decimal. When written, this register causes all 32 bits of the Access Data Register [access_data_byte[3:0]; 0x7C–0x7F] to be subsequently written to the selected equalizer microprogram store location within 2 symbol periods. Does not affect the value of the access data register. A factory-developed equalizer microcode is included with the no-fee licensed HDSL transceiver software available from Conexant.

7	6	5	4	3	2	1	0
—	—	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

0x7C–0x7F—Access Data Register (access_data_byte3:0)

A 4-byte read/write register that stores filter coefficient, equalizer register file, and equalizer microprogram store contents during indirect accesses to these RAM-based locations. Writes to addresses 0x70 through 0x7B, and uses the contents of this shared register as specified in each of the individual register descriptions.

4.0 Interconnection Information

NOTE: This section replaces the RS8973 Application Note (N8973AN1A).

The configuration described in this section supports data rates ranging from 144 kbps and 2320 kbps, with the output signal conforming to ETS TS 101 135 (formerly ETR 152) specifications for pulse-shape, power spectral density and output power at 784 kbps, 1168 kbps, and 2320 kbps.

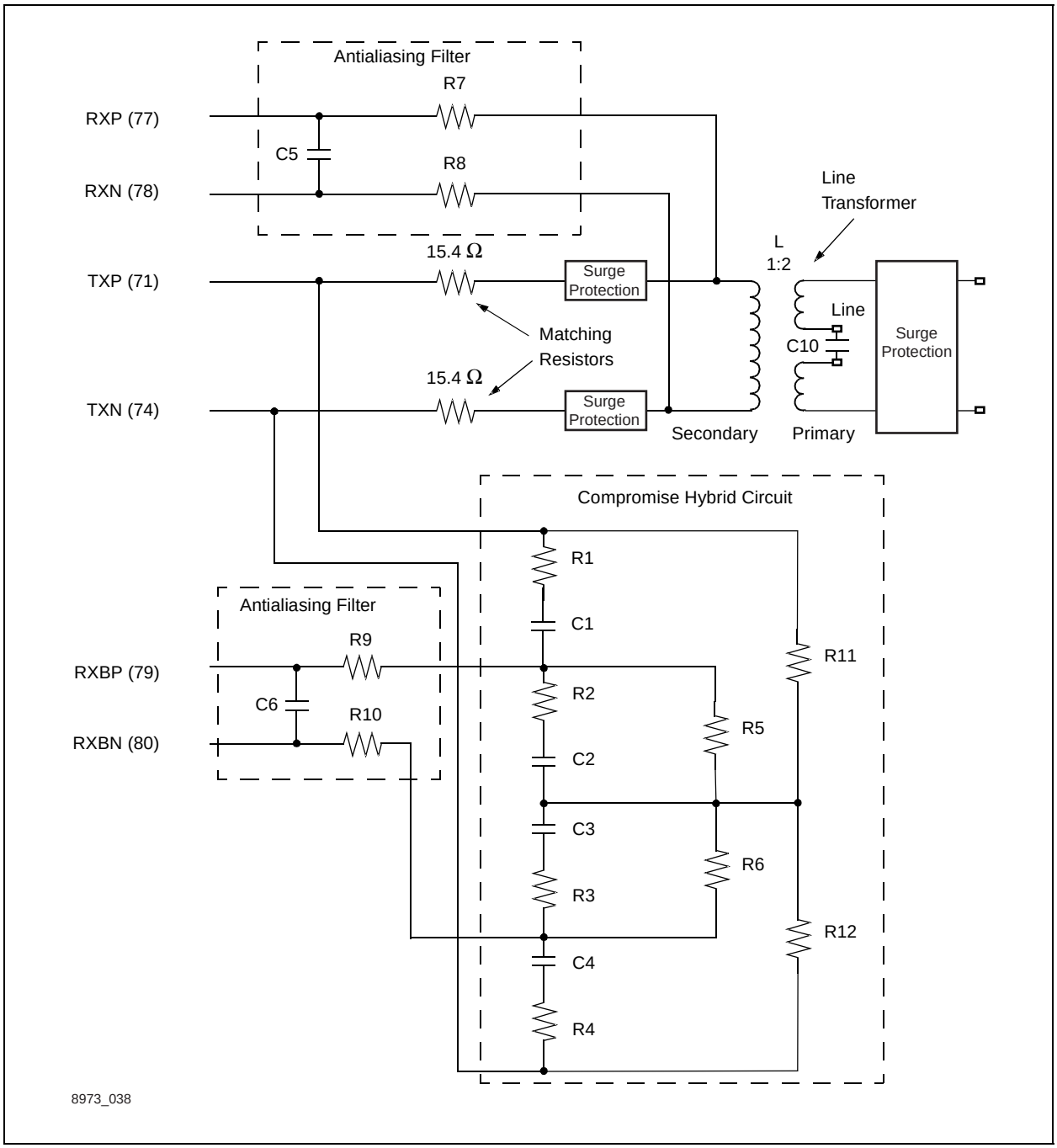
Four types of interconnections are discussed:

1. Transmission line interface, including the compromise hybrid
2. DC blocking capacitor
3. Voltage reference and compensation circuitry
4. Crystal/clock interface

4.1 Transmission Line Interface

The transmission line interface consists of the compromise hybrid, two impedance matching resistors and the line transformer. Figure 4-1, *Line Interface Interconnection Diagram*, illustrates the interconnections.

Figure 4-1. Line Interface Interconnection Diagram



4.1.1 Compromise Hybrid

The purpose of the compromise hybrid is to model the impedance of the transmission line. This model generates an approximation of the transmitted signal's echo. The echo replica is then subtracted from the signal on the line transformer to generate a first order approximation of the received signal. The RS8973 includes a dual differential analog input to accommodate a hybrid using only passive components.

Hybrid component values have been determined by means of calculations and simulations that optimize the echo cancellation functions at the frequencies of interest for the loops as specified in the ETS TS 101 135 (formerly ETR 152) standards. In addition, maximum reach was taken into consideration for the hybrid design.

To maximize digital echo cancellation within the RS8973, it is important that the compromise hybrid transfer function be highly linear. Therefore, we recommend that all capacitors used in the hybrid be NPO ceramic capacitors because of their highly linear characteristics.

Although the RS8973 contains a digital echo canceller (EC), the hybrid is needed to reduce the signal level input to the ADC. This eliminates ADC overflow for short loops and increases the resolution of the digitized receive signal for better digital signal processing performance. In addition, because the digital EC cannot cancel out very low frequency signals, it is very important that the analog EC cancel out most of the low frequency echo.

Table 4-1 lists compromise hybrid component values.

Table 4-1. Compromise Hybrid Component Values

Hybrid Components	Value
R1, R4	1.58 kΩ
C1, C4	2.3 nF
R2, R3	2.0 kΩ
C2, C3	1 nF
R5, R6	6.04 kΩ
R11, R12	5.1 kΩ

NOTE: All capacitors in the signal path should be film or NPO ceramic capacitors.

4.1.2 Impedance-Matching Resistors

Impedance-matching resistors are placed in the transmit path so that the output impedance of the line interface more closely matches the impedance of the transmission line and load. This maximizes the power transferred to the receiver on the other end of the line. The load is assumed to be 135 Ω.

Anti-aliasing filters are built on-chip to filter out high frequencies that would be aliased back into the passband as noise. These filters can be made of all passive components. The cutoff frequency (fc) should be as low as possible to achieve maximum attenuation of aliasing frequencies without filtering out the desired signal. Because the highest frequency in the desired signal is equal to one-half of the symbol rate, there should be no more than 1 dB of attenuation at this frequency. Table 4-2 lists the component values recommended for the antialiasing filters. Note that the other components in the hybrid affect the frequency response of the antialiasing filters.

Table 4-2. Antialias Filter Component Values

Antialias Filter Components	Value
R7, R8	1 kΩ
C5	56pF
R9, R10	1 kΩ
C6	56 pF

4.1.3 Line Transformer

The line transformer provides DC isolation from the transmission line by creating a high-pass filter. The winding ratio of the transformer must be 2:1 (line side:circuit side) to generate the appropriate voltage level on the line. The primary inductance (L) of the transformer (line side) is a very critical parameter. If L is too high, the cutoff frequency of the filter will be too low and the RS8973 Echo Canceller and Equalizer will not be able to cancel out the low frequency components of the echo and inter-symbol interference. If L is too low, part of the information in the signal will be filtered out, thereby decreasing the SNR ratio. In addition, the line transformer must meet other requirements to maximize system performance. See Table 4-3 for line transformer requirements.

Table 4-4 lists additional requirements that may be needed to specify the line transformer, depending upon the application in which it is to be used. These requirements have been submitted to several transformer vendors to expedite the development process. A list of these transformer vendors along with their associated transformer part numbers is listed in Table 4-5. These requirements may need to be modified to match the needs of a specific system. For example, if remote line powering is being used, the transformer must operate under a fairly high DC current condition. The exact current specification will depend on several factors including the voltage provided over the line, and the power consumption at the remote end. The application-specific requirements should be reviewed to ensure the transformer is not under- or over-specified. An over-specified transformer may unnecessarily increase cost, while an under-specified transformer may not perform adequately under all system conditions.

Table 4-3. Line Transformer Specifications

Parameter	Value
Turns Ratio(1)	2:1 (±2%)
Primary Inductance(2)	2 mH (±10%)
Return Loss (mid-band)	16 dB (40 to 300 kHz)
Return Loss (low-band)	–20 dB/decade (below 40 kHz)
Return Loss (high-band)	–20 dB/decade (above 300 kHz)
Longitudinal Balance (low-band)	53 dB (0.5 to 300 kHz)
Longitudinal Balance (high band)	–20 dB/decade (above 300 kHz)
Insertion Loss	0.5 dB at 40 kHz
Frequency Response	±0.1 dB (36 to 580 kHz)
Total Harmonic Distortion(3)	–70 dB at 36 kHz

NOTE(S):
(1) Turns ratio is specified line side to circuit side (line side:circuit side). The line side windings are usually split to accommodate a DC blocking capacitor.
(2) The primary inductance is for the line side of the transformer.
(3) Test condition: 14 dBm on line side (135 Ω load) with DC current present (if applicable).

Table 4-4. Line Transformer Application-Specific Specifications

Parameter	Requirement
Operating Temperature Range	–40 °C to +85 °C
DC Current	60 mA
Dielectric Strength	1500 VDC / 3000 VAC
Creepage and Clearance	—

Table 4-5. Recommended Line Transformer Suppliers

Supplier Name and Address	Supplier Phone Number(s)	Part Number
Midcom, Inc. P.O. Box 1330 Watertown, SD 57201	(800) 643-2661 (605) 886-4385	50050
Pulse Engineering Application Engineering 1220 World Trade Dr. San Diego, CA 92128	(619) 674-8100	—
Schott Corporation 1000 Parkers Lake Rd Minneapolis, MN 55391	(612) 475-1173	—

4.2 DC Blocking Capacitor

A DC blocking capacitor is placed in series with the center split primary winding (line side) of the line transformer to facilitate remote power feed or injection of sealing current. See Table 4-6.

Table 4-6. DC Blocking Capacitor Value

Component	Value
C10	1 µF

4.3 Voltage Reference and Compensation Circuitry

Compensation capacitors must be connected between all of the RS8973 voltage reference pins and analog ground. The voltage reference signals, their associated pin numbers, and the recommended compensation capacitor values are listed in Table 4-7.

Table 4-7. Compensation Capacitor Values

Signal Name	Pin Number	Capacitor Value
VCOMO	58	0.22 µF
VCOMI	57	0.22 µF
VCCAP	59	0.22 µF
VRXP	51	0.22 µF
VRXN	52	0.22 µF
VTXP	60	0.22 µF
VTXN	61	0.22 µF

In addition to the compensation capacitors, an external resistor is needed to set the bias current used in the RS8973. This resistor must be connected between the RBIAS pin (pin 56) and analog ground. The recommended value of the resistor is given in Table 4-8.

Table 4-8. Bias Current Resistor Value

Signal Name	Pin Number	Resistor Value
RBIAS	56	9.53 kΩ

4.4 Crystal/Clock Interface

A crystal or an external clock is needed to provide a reference clock for the RS8973. If a crystal is used, it must be connected to the XTALI/MCLK and XTALO pins along with two external capacitors as shown in Figure 4-2. The recommended specification for the crystal is given in Table 4-9. A list of crystal vendors and their associated part numbers is displayed in Table 4-10.

If an external clock is used, it must be connected to the XTALI/MCLK pin (pin 40), and the XTALO pin (pin 39) must be left floating. The clock frequency must be 10.24 MHz.

Figure 4-2. Crystal Oscillator Connection Diagram

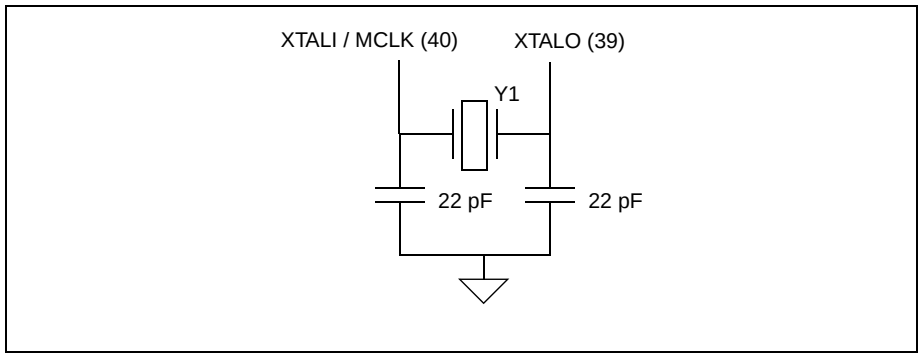


Table 4-9. Crystal Specification

Parameter	Value
Nominal Frequency	10.24 MHz
Frequency Tolerance at 25 °C	±10 ppm
Temperature Frequency Stability	±10 ppm
Aging	±10 ppm over 10 years
Load Capacitance	15.5 pF
NOTE(S): Individual frequency tolerance, temperature frequency stability, and aging requirements can vary as long as the total tolerance is less than ±30 ppm.	

Table 4-10. Recommended Crystal Suppliers

Supplier Name and Address	Supplier Phone Number	Part Number
Ecliptek Corporation 3545 Cadillac Avenue Costa Mesa, CA 92626	(714) 433-1200	ECX-5173-10.240M
General Electronic Devices 320 S. Pacific Street San Marcos, CA 92069	(760) 591-4170	HC49-10.240- .0155- .001/01

5.0 Electrical and Mechanical Specifications

5.1 Absolute Maximum Ratings

Stresses above those listed in Table 5-1 may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
V_{Supply}	Supply voltage(1)–VDD2, VPLL, VAA	–0.5	+7	V
V_{Supply}	Supply voltage(1)–VDD1	–0.5	4.6	V
V_I	Input voltage on any signal pin(2)	–0.5	V_{DD2} + 0.5	V
T_{ST}	Storage temperature	–65	+125	°C
T_{VSOL}	Vapor-phase soldering temperature (1 minute)	—	+220	°C

NOTE(S):
(1) V_{DD1}, V_{DD2}, relative to DGND. V_{AA} relative to AGND.
(2) Relative to DGND.

5.2 Recommended Operating Conditions

The recommended operating conditions are described in Table 5-2.

Table 5-2. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{DD1}	Digital core-logic supply voltage	3.0	3.3	3.6	V
V_{DD2}	Digital I/O-buffer supply voltage	4.75	5.0	5.25	V
V_{AA}	Analog supply voltage	4.75	5.0	5.25	V
V_{PLL}	PLL supply voltage	4.75	5.0	5.25	V
V_{IH}	High-level input voltage (1)	2.0	—	V_{DD2} + 0.3	V
V_{IL}	Low-level input voltage	–0.3	—	+0.8	V
V_{IHX}	High-level input voltage for XTALI / MCLK	0.9 × V_{DD2}	—	V_{DD2} + 0.3	V
V_{ILX}	Low-level input voltage for XTALI / MCLK	–0.3	—	0.1 × V_{DD2}	V
C_L	Output capacitive loading(2)	—	—	60	pF
T_A	Ambient operating temperature(3)	–40	—	+85	°C

(1) V_{IH} (minimum) for the following inputs is 2.2 volts:
$\overline{WR}$/R/$\overline{W}$ RBCLK
$\overline{RST}$ TBCLK
(2) Capacitive loading over which all digital output switching characteristics are guaranteed.
(3) Still-air temperature range over which all electrical characteristics and timing requirements/characteristics are guaranteed.

5.3 Electrical Characteristics

Typical characteristics measured at nominal operating conditions:

- T_A = 25 °C
- V_{DD1} = 3.3 V
- $V_{DD2/AA/PLL}$ = 5.0 V

Minimum/maximum characteristics guaranteed over extreme operating conditions:

- Min ≤ T_A ≤ max
- Min ≤ $V_{DD/AA}$ ≤ max

The parameters of the electrical characteristics are displayed in Table 5-3.

Table 5-3. Electrical Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{OH}	High-Level Output Voltage @ I_{OH} = – 400 µA	2.4	—	—	V
V_{OLL}	Low-Level Output Voltage @ I_{OL} = 6 mA ($\overline{IRQ}$ and $\overline{READY}$)	—	—	0.4	V
V_{OL}	Low-Level Output Voltage @ I_{OL} = 3 mA (All Other Outputs)	—	—	0.4	V
I_I	Input Leakage Current @ $V_{SS2} \le V_I \le V_{DD2}$	—	—	±10	µA
I_{OZ}	High-Impedance Output Leakage Current @ $V_{SS2} \le V_O \le V_{DD2}$	—	—	±10	µA
I_{PR}	Resistive Pull-Up Current @ $V_I = V_{SS2}$ (TDI and TMS)	–20	—	–400	µA
I_{5V}	5 V Supply Current @ F_{QCLK} = 72 kHz(1)	—	100	TBD	mA
I_{5V}	5 V Supply Current @ F_{QCLK} = 392 kHz(1)	—	101	TBD	mA
I_{5V}	5 V Supply Current @ F_{QCLK} = 584 kHz(1)	—	102	TBD	mA
I_{5V}	5 V Supply Current @ F_{QCLK} = 776 kHz(1)	—	103	TBD	mA
I_{5V}	5 V Supply Current @ F_{QCLK} = 1160 kHz(1)	—	105	TBD	mA
I_{3V}	3.3 V Supply Current @ F_{QCLK} = 72 kHz(2)	—	25	TBD	mA
I_{3V}	3.3 V Supply Current @ F_{QCLK} = 392 kHz(2)	—	54	TBD	mA
I_{3V}	3.3 V Supply Current @ F_{QCLK} = 584 kHz(2)	—	70	TBD	mA
I_{3V}	3.3 V Supply Current @ F_{QCLK} = 776 kHz(2)	—	87	TBD	mA
I_{3V}	3.3 V Supply Current @ F_{QCLK} = 1160 kHz(2)	—	120	TBD	mA
I_{PD5V}	Power-Down Current @ F_{QCLK} = 72 kHz(3)	—	15	TBD	mA
I_{PD5V}	Power-Down Current @ F_{QCLK} = 1160 kHz(3)	—	18	TBD	mA
I_{PD3V}	Power-Down Current @ F_{QCLK} = 72 kHz(4)	—	1	TBD	mA
I_{PD3V}	Power-Down Current @ F_{QCLK} = 1160 kHz(4)	—	1	TBD	mA
C_I	Input Capacitance	—	—	10	pF
C_{OZ}	High-Impedance Output Capacitance	—	—	10	pF

NOTE(S):
(1) $I_{5V} = I_{PLL} + I_{DD2} + I_{AA}$ during normal operation.
(2) $I_{3V} = I_{DD1}$ during normal operation.
(3) $I_{PD5V} = I_{PLL} + I_{DD2} + I_{AA}$ during power-down operation.
(4) $I_{PD3V} = I_{DD1}$ during power-down operation.

5.4 Clock Timing

Tables 5-4 through 5-6 list the clock timing requirements and switching characteristics. Figures 5-1 and 5-2 illustrate MCLK timing requirements and clock control timing, respectively.

Table 5-4. MCLK Timing Requirements

Symbol	Parameter	Minimum	Typical	Maximum	Units
1	MCLK Period(1)	97.653	97.656	97.659	ns
2	MCLK Pulse-Width Low	35	—	—	ns
3	MCLK Pulse-Width High	35	—	—	ns

NOTE(S):
(1) If an external clock is applied to XTALI/MCLK, it is referred to as MCLK. Max tolerance = ± 32 ppm.
Edge rates for MCLK are < 5 ns.

Figure 5-1. MCLK Timing Requirements

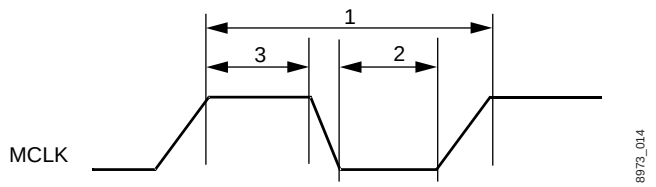


Table 5-5. HCLK Switching Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
4	HCLK Period (T_{HCLK}), hclk_freq[1:0] = '11'(1)	$T_{QCLK} \div 64$	$T_{QCLK} \div 64$	$T_{QCLK} \div 64$	—
5	HCLK Period (T_{HCLK}), hclk_freq[1:0] = '00' or '01'(1)	$T_{QCLK} \div 16$	$T_{QCLK} \div 16$	$T_{QCLK} \div 16$	—
6	HCLK Period (T_{HCLK}), hclk_freq[1:0] = '10'(1)	$T_{QCLK} \div 32$	$T_{QCLK} \div 32$	$T_{QCLK} \div 32$	—
7	HCLK Pulse-Width High	$T_{HCLK} \div 2 - 10$	$T_{HCLK} \div 2$	$T_{HCLK} \div 2 + 10$	ns
8	HCLK Pulse-Width Low	$T_{HCLK} \div 2 - 10$	$T_{HCLK} \div 2$	$T_{HCLK} \div 2 + 10$	ns

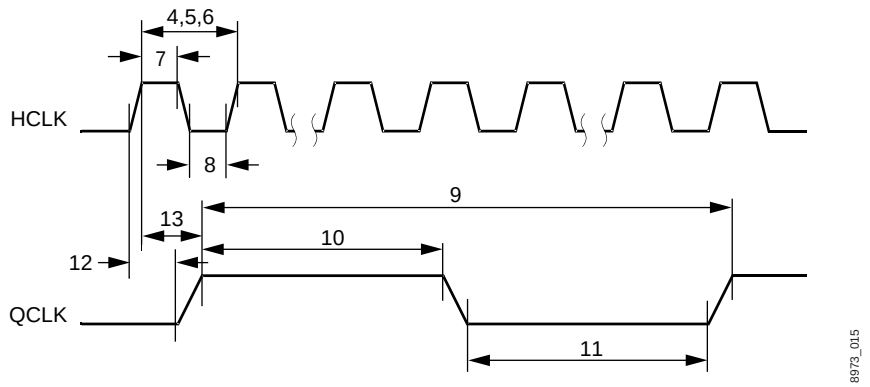
NOTE(S):
(1) The hclk_freq[1:0] control bits are located in the Serial Monitor Source Select Register [addr. 0x01].

Table 5-6. QCLK Switching Characteristics

Symbol	Parameter	Minimum	Maximum	Units
9	QCLK period (T_{QCLK})(1)	—	—	
10	QCLK pulse-width high	$T_{QCLK} \div 2 - 20$	$T_{QCLK} \div 2 + 20$	ns
11	QCLK pulse-width low	$T_{QCLK} \div 2 - 20$	$T_{QCLK} \div 2 + 20$	ns
12	QCLK hold after HCLK rising edge	–20		ns
13	QCLK delay after HCLK high	—	20	ns

NOTE(S):
(1) T_{QCLK} is defined as the time period of the symbol rate. The symbol rate is data rate ÷ 2.

Figure 5-2. Clock Control Timing



5.5 Channel Unit Interface Timing

Tables 5-7 through 5-12 list channel unit interface timing requirements and switching characteristics. Figures 5-3 through 5-5 illustrate channel unit interface timing in parallel master mode, parallel slave mode, and serial mode, respectively.

Table 5-7. Channel Unit Interface Timing Requirements, Parallel Master Mode

Symbol	Parameter	Minimum	Maximum	Units
14	TQ[1,0] setup prior to QCLK falling edge	100	—	ns
15	TQ[1,0] hold after QCLK low	25	—	ns

Table 5-8. Channel Unit Interface Switching Characteristics, Parallel Master Mode

Symbol	Parameter	Minimum	Maximum	Units
16	RQ[1,0] hold after QCLK rising edge	–50	—	ns
17	RQ[1,0] delay after QCLK high	—	50	ns

Figure 5-3. Channel Unit Interface Timing, Parallel Master Mode

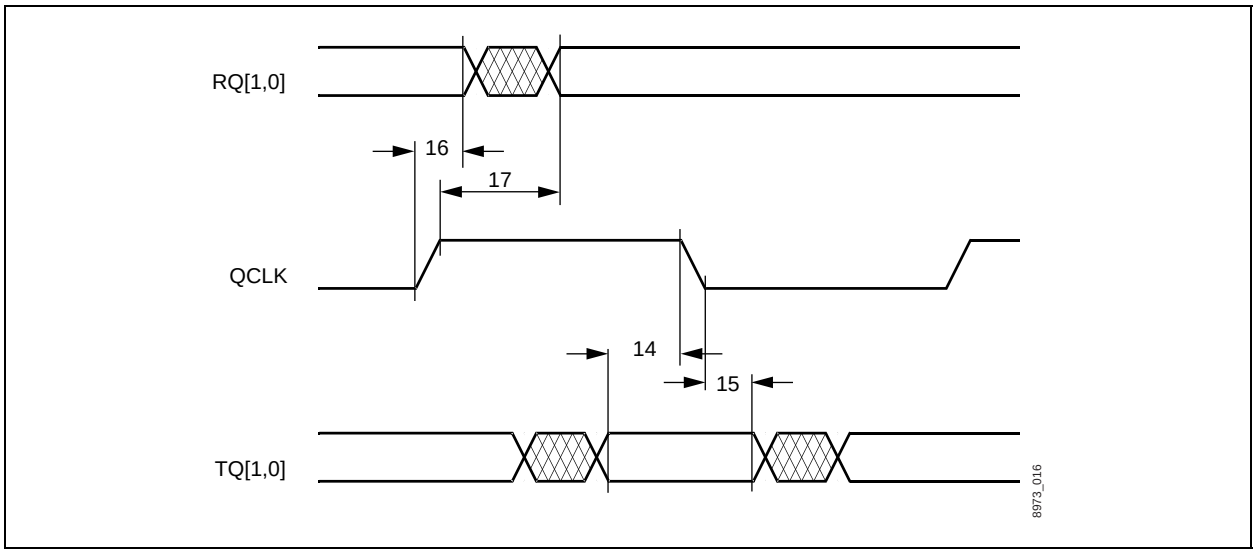


Table 5-9. Channel Unit Interface Timing Requirements, Parallel Slave Mode

Symbol	Parameter	Minimum	Maximum	Units
18	TBCLK, RBCLK Period(1)	T_{QCLK}	T_{QCLK}	—
19	TBCLK, RBCLK Pulse-Width High	$T_{QCLK} \div 4$	—	—
20	TBCLK, RBCLK Pulse-Width Low	$T_{QCLK} \div 4$	—	—
21	TQ[1,0] Setup prior to TBCLK Active Edge(2)	25	—	ns
22	TQ[1,0] Hold after TBCLK High/Low(2)	25	—	ns

NOTE(S):
(1) TBCLK and RBCLK must be frequency-locked to QCLK, though they may have independent phase relationships to QCLK and to one another.
(2) TBCLK polarity (edge sensitivity) is programmable through the CU Interface Modes Register [cu_interface_modes 0x06].

Table 5-10. Channel Unit Interface Switching Characteristics, Parallel Slave Mode

Symbol	Parameter	Minimum	Maximum	Units
23	RQ[1,0] hold after RBCLK active edge(1)	0	—	ns
24	RQ[1,0] delay after RBCLK high/low(1)	—	100	ns

NOTE(S):
(1) RBCLK polarity (edge sensitivity) is programmable through the CU Interface Modes Register [cu_interface_modes; 0x06].

Figure 5-4. Channel Unit Interface Timing, Parallel Slave Mode

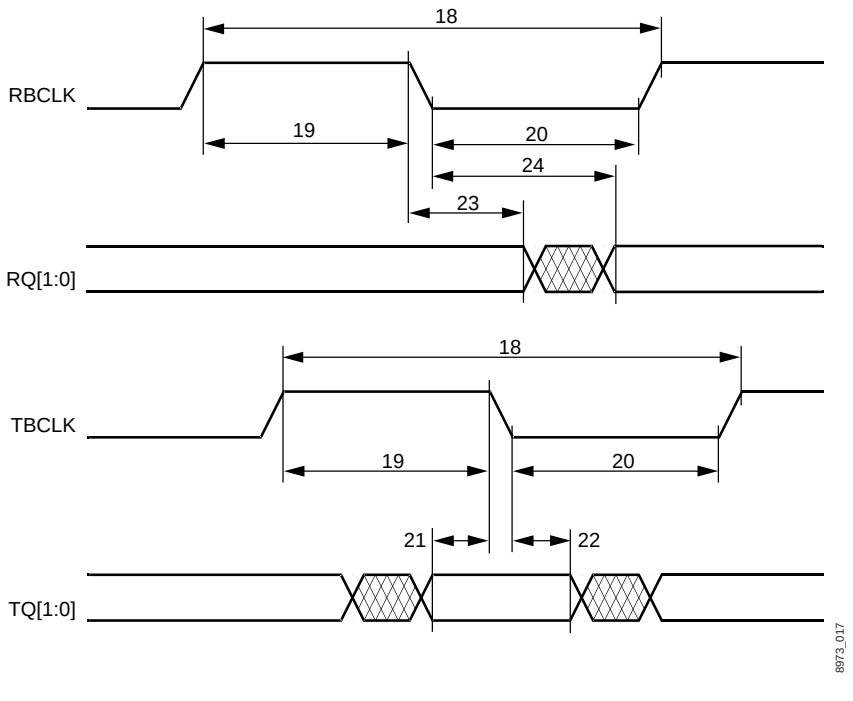


Figure 5-4. Channel Unit Interface Timing, Parallel Slave Mode

> ***NOTE(S):*** TBCLK and RBCLK polarities are programmable through the CU Interface Modes Register. The figure depicts both clocks programmed to falling-edge active.

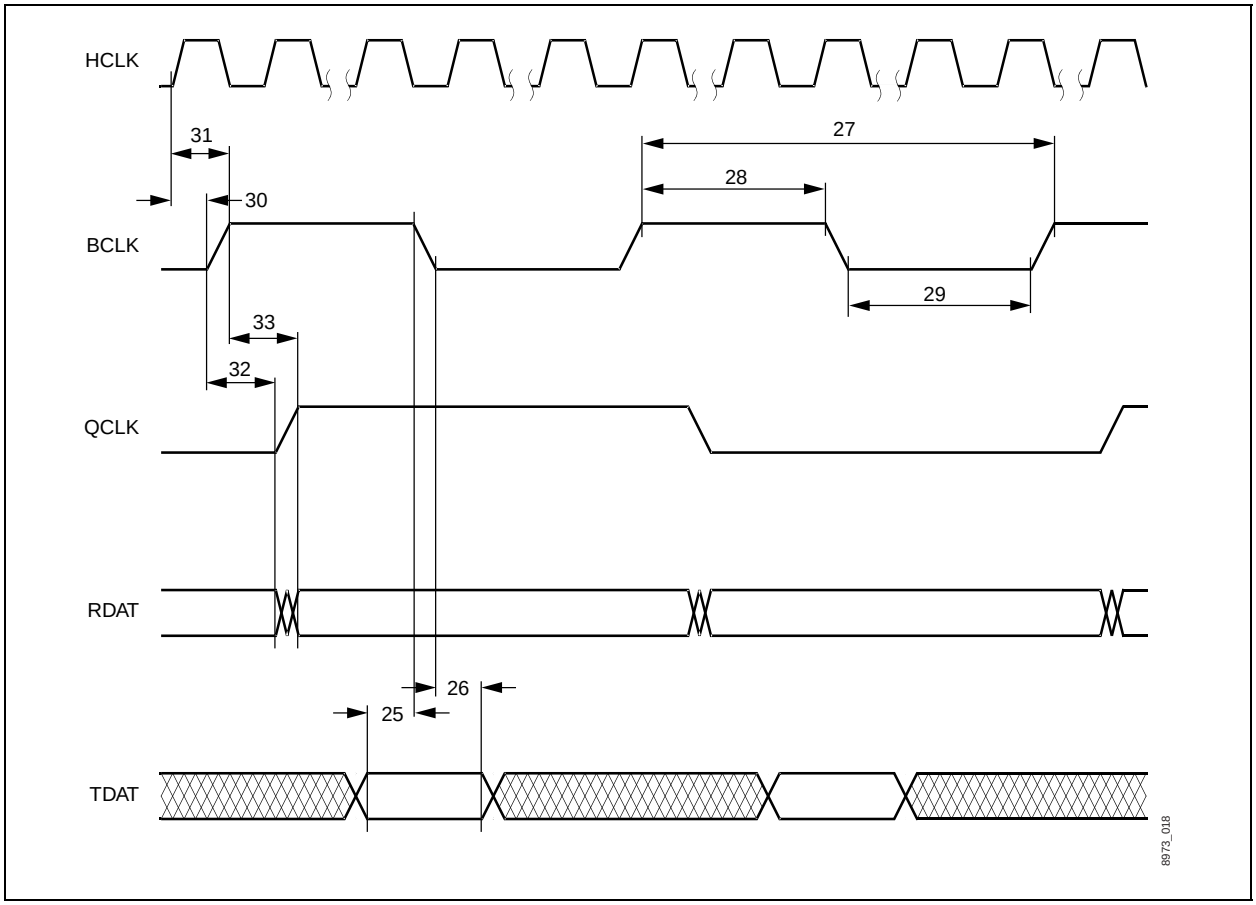
Table 5-11. Channel Unit Interface Timing Requirements, Serial Mode

Symbol	Parameter	Minimum	Maximum	Units
25	TDAT setup prior to BCLK falling edge	100	—	ns
26	TDAT hold after BCLK low	25	—	ns

Table 5-12. Channel Unit Interface Switching Characteristics, Serial Mode

Symbol	Parameter	Minimum	Maximum	Units
27	BCLK period	$T_{QCLK} \div 2$	$T_{QCLK} \div 2$	—
28	BCLK pulse-width high	$T_{QCLK} \div 4 - 20$	$T_{QCLK} \div 4 + 20$	ns
29	BCLK pulse-width low	$T_{QCLK} \div 4 - 20$	$T_{QCLK} \div 4 + 20$	ns
30	BCLK hold after HCLK rising edge	0	—	ns
31	BCLK delay after HCLK high	—	50	ns
32	RDAT, QCLK hold after BCLK rising edge	–50	—	ns
33	RDAT, QCLK delay after BCLK high	—	50	ns

Figure 5-5. Channel Unit Interface Timing, Serial Mode



5.6 Microcomputer Interface Timing

Tables 5-13 and 5-14 list microcomputer interface (MCI) timing requirements and switching characteristics, respectively. Figures 5-6 through 5-9 illustrate MCI write and read timing. Figure 5-10 illustrates internal write timing.

Table 5-13. Microcomputer Interface Timing Requirements

Symbol	Parameter	Minimum	Maximum	Units
34	ALE pulse-width high	30	—	ns
35	Address setup prior to ALE falling edge(1)	10	—	ns
36	Address hold after ALE low(1)	5	—	ns
37	ALE low prior to $\overline{\text{Write Strobe}}$ falling edge(2)	20	—	ns
38a	$\overline{\text{Read Strobe}}$ falling edge after ALE falling edge – muxed mode (MUXED = 1)(3)	20	—	ns
38b	$\overline{\text{Read Strobe}}$ falling edge after ALE falling edge – non-muxed mode (MUXED = 0)(3)	1	—	ns
39	$\overline{\text{Write Strobe}}$ pulse-width low(2,4)	$T_{QCLK} \div 32 + 25$	—	ns
40	$\overline{\text{Read Strobe}}$ pulse-width low(3,4)	$T_{QCLK} \div 32 + 25$	—	ns
41	Data In setup prior to $\overline{\text{Write Strobe}}$ rising edge(2)	30	—	ns
42	Data In hold after $\overline{\text{Write Strobe}}$ high(2)	5	—	ns
43	R/$\overline{\text{W}}$ setup prior to $\overline{\text{Read/Write Strobe}}$ falling edge	10	—	ns
44	R/$\overline{\text{W}}$ hold after $\overline{\text{Read/Write Strobe}}$ high	10	—	ns
45	ALE falling edge after $\overline{\text{Write Strobe}}$ high	20	—	ns
46	ALE falling edge after $\overline{\text{Read Strobe}}$ high	20	—	ns
47	$\overline{\text{RST}}$ pulse-width low	50	—	ns
48	$\overline{\text{Write Strobe}}$ rising edge after $\overline{\text{READY}}$ low	0	—	ns

NOTE(S):
(1) Address is defined as AD[7:0] when MUXED = 1, and ADDR[7:0] when MUXED = 0.
(2) In Intel mode, $\overline{\text{Write Strobe}}$ is defined as $\overline{\text{WR}}$ and $\overline{\text{CS}}$ asserted. In Motorola mode, it is defined as $\overline{\text{DS}}$ and $\overline{\text{CS}}$ asserted when R/$\overline{\text{W}}$ is low.
(3) In Intel mode, $\overline{\text{Read Strobe}}$ is defined as $\overline{\text{RD}}$ and $\overline{\text{CS}}$ asserted. In Motorola mode, it is defined as $\overline{\text{DS}}$ and $\overline{\text{CS}}$ asserted when R/$\overline{\text{W}}$ is high.
(4) The timing listed is for the synchronous mode of the MCI, which is power-on default. It can also be set to asynchronous mode by setting bit 0 of the miscellaneous/test register (address 0x0F) to a 1. In this case, the minimum timing changes to 40 ns for symbol 39, and 50 ns for symbols 40 and 50. Synchronous mode is preferred because it reduces switching noise. To switch to asynchronous mode, the $\overline{\text{Write Strobe}}$ pulse-width (symbol 39) should meet the synchronous mode timing requirements for a symbol rate of 640 kbps (74 nx), which is the power-on default.

Table 5-14. Microcomputer Interface Switching Characteristics

Symbol	Parameter	Minimum	Maximum	Units
49	Data out enable (Low Z) after $\overline{\text{Read Strobe}}$ falling edge(1)	2	—	ns
50	Data out valid after $\overline{\text{Read Strobe}}$ low(1, 7)	—	$T_{QCLK} \div 32 + 25$	ns
51	Data out hold after $\overline{\text{Read Strobe}}$ rising edge(1)	2	—	ns
52	Data out disable (High Z) after $\overline{\text{Read Strobe}}$ high(1)	—	25	ns
53	$\overline{\text{IRQ}}$ hold after $\overline{\text{Write Strobe}}$ rising edge(2,3)	5	—	ns
54	$\overline{\text{IRQ}}$ delay after $\overline{\text{Write Strobe}}$ high(2,3)	—	$T_{QCLK} \div 32 + 20$	ns
55	Internal register delay after $\overline{\text{Write Strobe}}$ high(3,4)	—	$T_{QCLK} \div 32$	ns
56	Internal RAM delay after $\overline{\text{Write Strobe}}$ high(3,5)	—	$2 \times T_{QCLK}$	ns
57	Access data register delay after $\overline{\text{Write Strobe}}$ high(3,6)	—	$2 \times T_{QCLK}$	ns
58	$\overline{\text{READY}}$ low after $\overline{\text{Write Strobe}}$ low(3)	0	$T_{QCLK} \div 32$	ns
59	$\overline{\text{READY}}$ rising edge after $\overline{\text{Write Strobe}}$ high(3)	0	50	ns
60	$\overline{\text{READY}}$ low after $\overline{\text{Read Strobe}}$ low(1)	0	$T_{QCLK} \div 32$	ns
61	$\overline{\text{READY}}$ rising edge after $\overline{\text{Read Strobe}}$ high(1)	0	50	ns
62	Data out valid after $\overline{\text{READY}}$ low	—	10	ns

NOTE(S):

(1) $\overline{\text{Read Strobe}}$ is defined as $\overline{\text{RD}}$ and $\overline{\text{CS}}$ asserted in Intel mode, and $\overline{\text{DS}}$ and $\overline{\text{CS}}$ asserted when R/$\overline{\text{W}}$ is high in Motorola mode.

(2) When writing an interrupt mask or status register.

(3) $\overline{\text{Write Strobe}}$ is defined as $\overline{\text{WR}}$ and $\overline{\text{CS}}$ asserted in Intel mode, and $\overline{\text{DS}}$ and $\overline{\text{CS}}$ asserted when R/$\overline{\text{W}}$ is low in Motorola mode.

(4) Writes to internal registers are synchronized to an internal 64-times symbol-rate clock. Data is available for reading after the specified time. This parameter may extend the overall read access time from internal register locations under high bus speed/low symbol rate conditions.

(5) When performing an indirect write to RAM-based locations using a write select register [odd addresses: 0x71–0x7B] and the Access Data Register. Subsequent writes to any read/write select register or the Access Data Register, as initiated by a $\overline{\text{Write Strobe}}$ falling edge, is prohibited for the specified time. This parameter will extend the overall write access time to RAM-based locations under normal bus speed/symbol rate conditions.

(6) When performing an indirect read from RAM-based locations using a read select register [even addresses: 0x70–0x7A] and the Access Data Register. Subsequent writes to any read/write select register, as initiated by a $\overline{\text{Write Strobe}}$ falling-edge, is prohibited for the specified time. Data is available for reading from the Access Data Register after the specified time. This parameter will extend the overall read access time from RAM-based locations under normal bus speed/symbol rate conditions. Direct writes to the Access Data Register are as specified for internal registers.

(7) The timing listed is for the synchronous mode of the MCI, which is power-on default. It can also be set to asynchronous mode by setting bit 0 of the reserved9 register (address 0x0F) to a 1. In this case, the minimum timing changes to 40 ns for symbol 39, and 50 ns for symbols 40 and 50. Synchronous mode is preferred because it reduces switching noise. To switch to asynchronous mode, the $\overline{\text{Write Strobe}}$ pulse-width (symbol 39) should meet the synchronous mode timing requirements for a symbol rate of 640 kbps (74 nx), which is the power-on default.

Figure 5-6. MCI Write Timing, Intel Mode (MOTEL = 0)

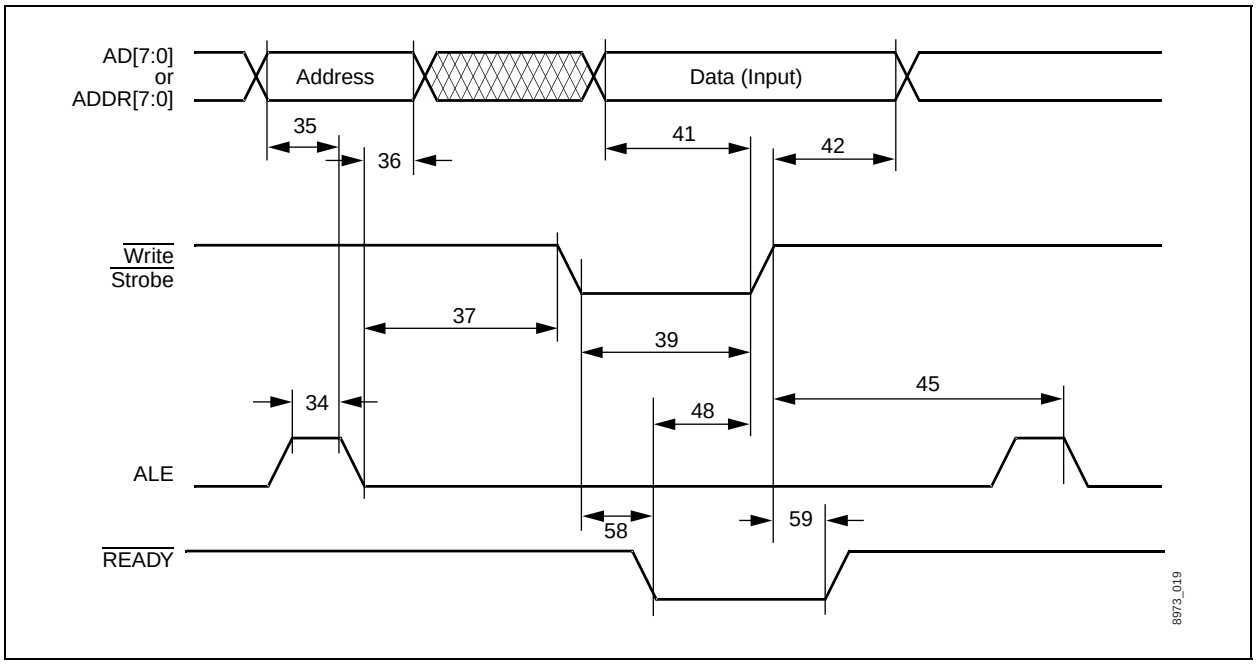


Figure 5-7. MCI Write Timing, Motorola Mode (MOTEL = 1)

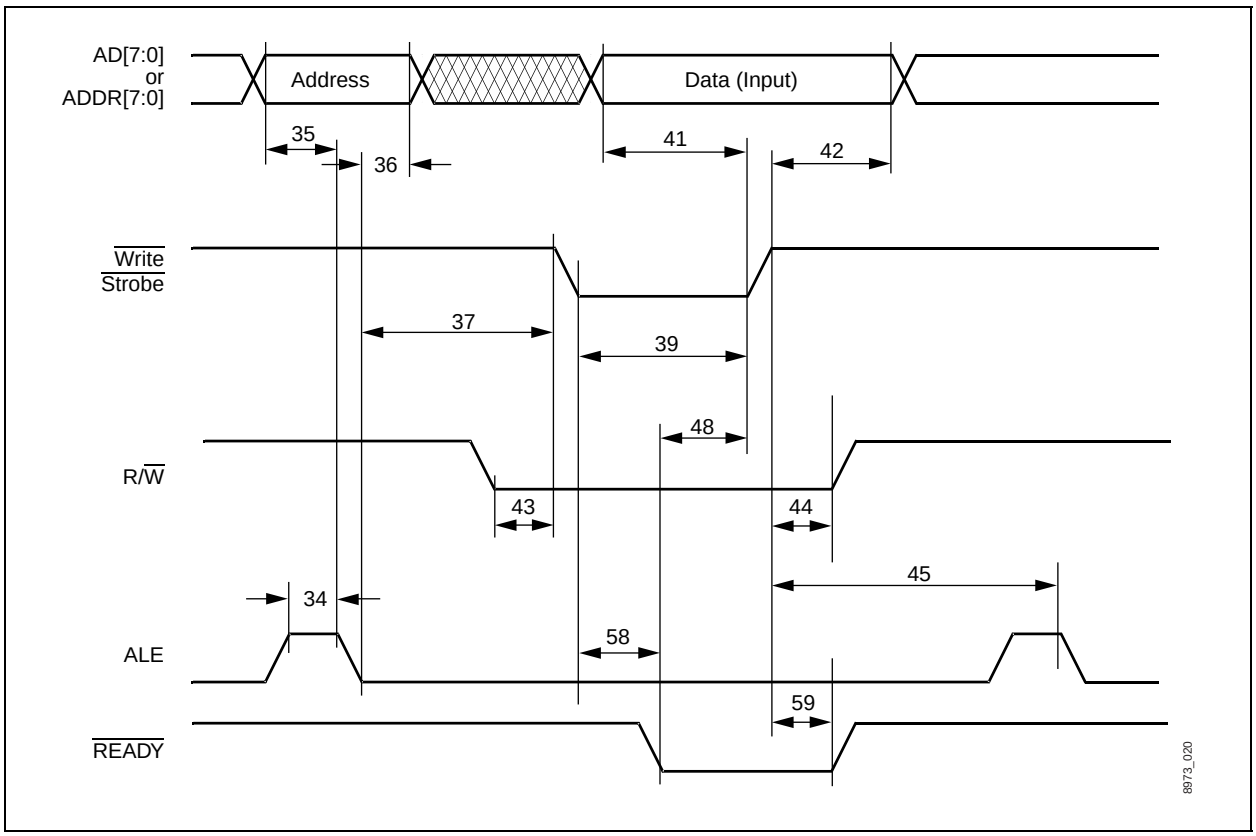


Figure 5-8. MCI Read Timing, Intel Mode (MOTEL = 0)

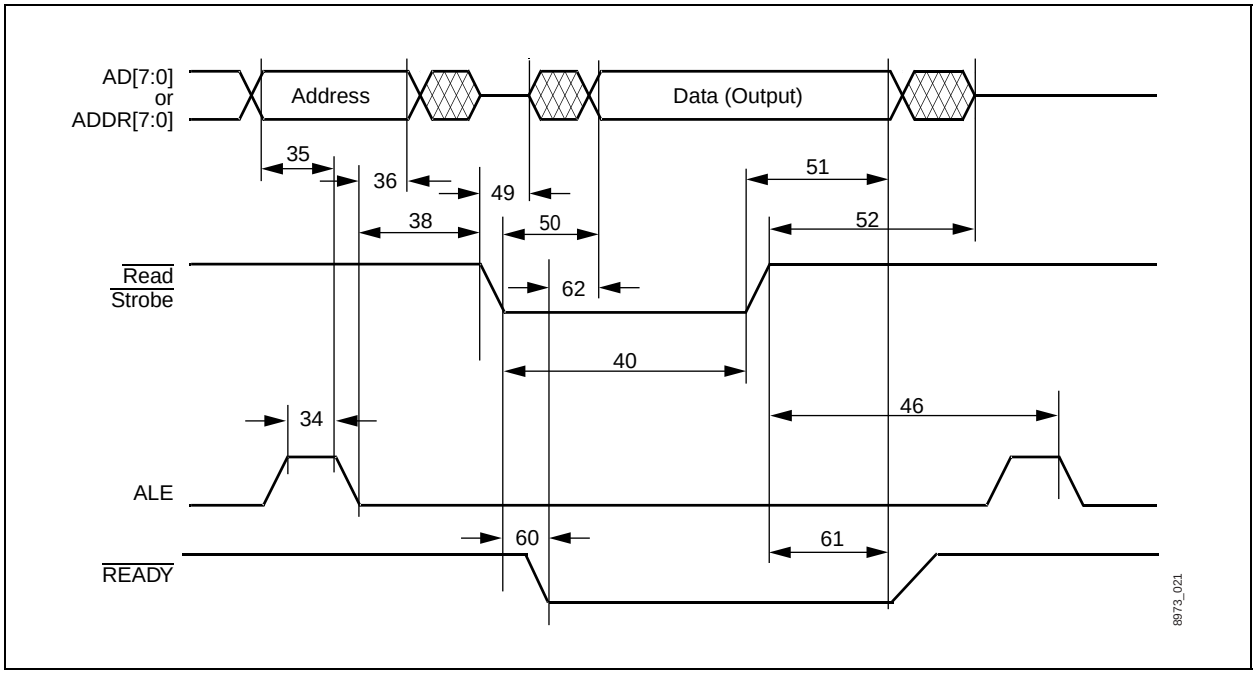


Figure 5-9. MCI Read Timing, Motorola Mode (MOTEL = 1)

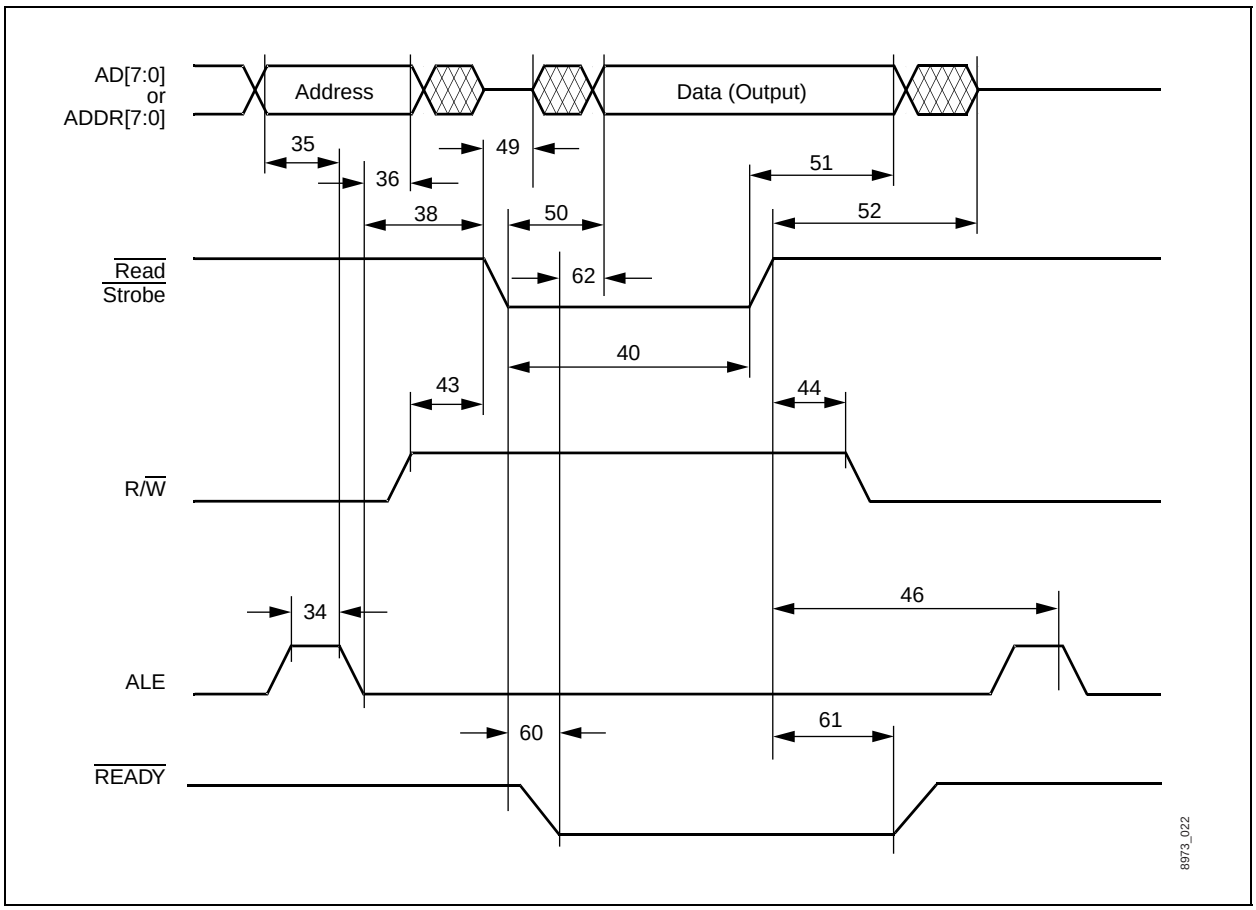
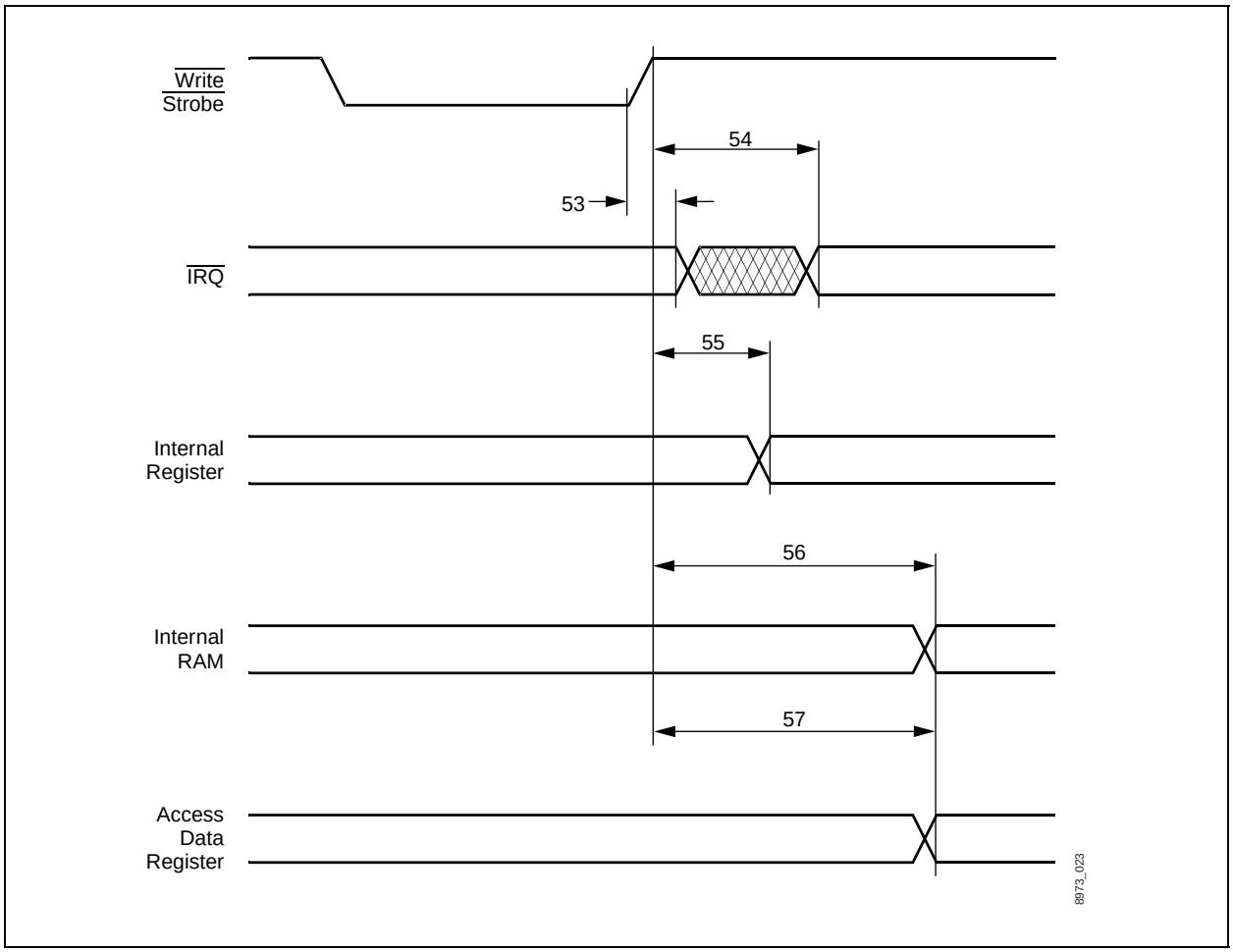


Figure 5-10. Internal Write Timing



5.7 Test and Diagnostic Interface Timing

Tables 5-15 and 5-16 list test and diagnostic interface timing requirements and switching characteristics. Figures 5-11 and 5-12 illustrate JTAG interface and SMON timing, respectively.

Table 5-15. Test and Diagnostic Interface Timing Requirements

Symbol	Parameter	Minimum	Maximum	Units
63	TCK pulse-width high	80	—	ns
64	TCK pulse-width low	80	—	ns
65	TMS, TDI setup prior to TCK rising edge(1)	20	—	ns
66	TMS, TDI hold after TCK high(1)	20	—	ns

NOTE(S):
(1) Also applies to functional inputs for SAMPLE/PRELOAD and EXTEST instructions.

Table 5-16. Test and Diagnostic Interface Switching Characteristics

Symbol	Parameter	Minimum	Maximum	Units
67	TDO hold after TCK falling edge(1)	0	—	ns
68	TDO delay after TCK low(1)	—	50	ns
69	TDO enable (Low Z) after TCK falling edge(1)	2	—	ns
70	TDO disable (High Z) after TCK low(1)	—	25	ns
71	SMON hold after HCLK rising edge(2)	0	—	ns
72	SMON delay after HCLK high(2)	—	50	ns

NOTE(S):
(1) Also applies to functional outputs for the EXTEST instruction.
(2) HCLK must be programmed to operate at 16 times the symbol rate (16 × F_{QCLK}).

Figure 5-11. JTAG Interface Timing

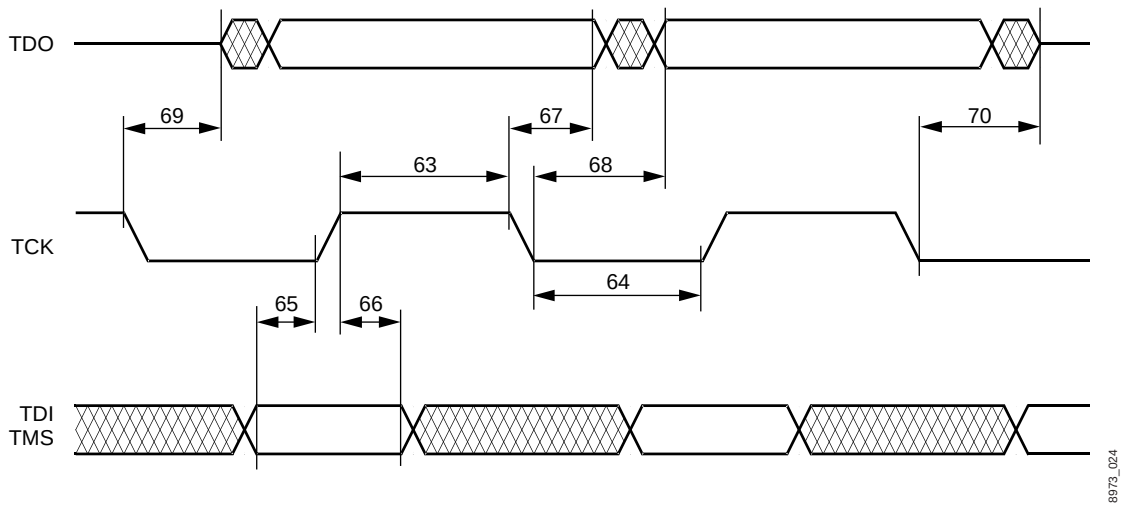
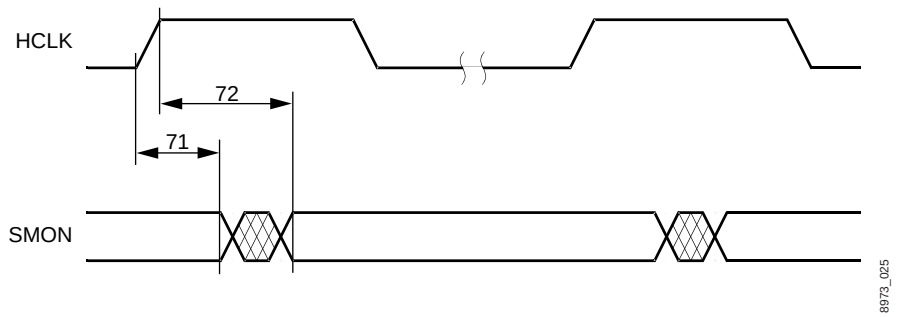


Figure 5-12. SMON Timing



5.8 Analog Specifications

Tables 5-17 and 5-18 list transmitter and receiver analog requirements and specifications. Figure 5-13 and Table 5-19 show the transmit pulse template for two- and three-pair systems. Figure 5-14 and Table 5-20 show the transmit pulse template for one-pair systems. Figures 5-15 through 5-17 illustrate the upper bound of the average PSD of 392, 584, and 1160 kbaud systems, respectively.

Table 5-17. Receiver Requirements and Specifications

Parameter	Comments	Min	Typ	Max	Units
Input signals	RXP, RXN, RXBP, and RXBN	—	—	—	—
Input voltage range	With respect to VAA/2	–2.25	—	+2.25	V
Input resistance	@ Data Rate = 2320 kbps	—	10	—	kΩ
Input resistance	@ Data Rate = 144 kbps	—	35	—	kΩ
Common mode voltage	VCOMI	—	VAA × 0.4	—	V
VGA	Six gains from 0 dB to +15 dB	—	—	—	—
Gain step	—	2.55	3.0	3.42	dB
ADC	—	—	—	—	—
Differential voltage range (full scale input, FS)(1)	$(V_{RXP} – V_{RXN})—(V_{RXBP} – V_{RXBN})$	5.4	6.0	6.6	V_P
Timing recovery PLL pull-in range (digital)	—	±64	—	—	ppm
PLL settling time	—	—	10	—	ms

NOTE(S):
(1) Corresponds to the voltages that produce a full scale reading from the ADC when the VGA gain equals O dB. The input voltage range is reduced proportionally as VGA gain is increased.

Table 5-18. Transmitter Analog Requirements and Specifications *(1 of 2)*

Parameter	Comments	Min	Typ	Max	Units
Transmit symbol rate (f_{qclk})	QCLK frequency (data rate/2)	72	—	1160	kHz
Pulse template(1, 2, 3)	See Figure 5-13 and Figure 5-14, R_L = 135 Ω	—	—	—	—

Table 5-18. Transmitter Analog Requirements and Specifications *(2 of 2)*

Parameter	Comments	Min	Typ	Max	Units
Power spectral density(1, 2, 3,4)	See Figures 5-15, 5-16 and 5-17, R_L = 135 Ω	—	—	—	—
Average power(1, 2, 3,4)	DC to 2 x F_{QCLK}, R_L = 135 Ω, calibrated gain setting	13.4	—	14	dBm
Gain adjustment step	Controlled by Transmit Gain Register [0x29]	—	0.20	—	dB
Common-mode voltage	VCOMO	—	VAA/2	—	V
Output impedance(1)	DC to 1 MHz	—	—	2	Ω

NOTE(S):
(1) Guaranteed by design and characterization.
(2) See Figure 5-18 of Section 5.9, *Test Conditions*, for the test circuit.
(3) Measured after the transmitter is calibrated by writing the value in the Transmitter Calibration Register [tx_calibrate; 0x28] to the Transmitter Gain Register [tx_gain; 0x29].
(4) Measured with a pseudo-random code sequence of pulses.

Figure 5-13. Transmit Pulse Template for Two- and Three-Pair Systems; Normalized Pulse Mask (Source ETSI TS 101 135 Formerly ETR 152)

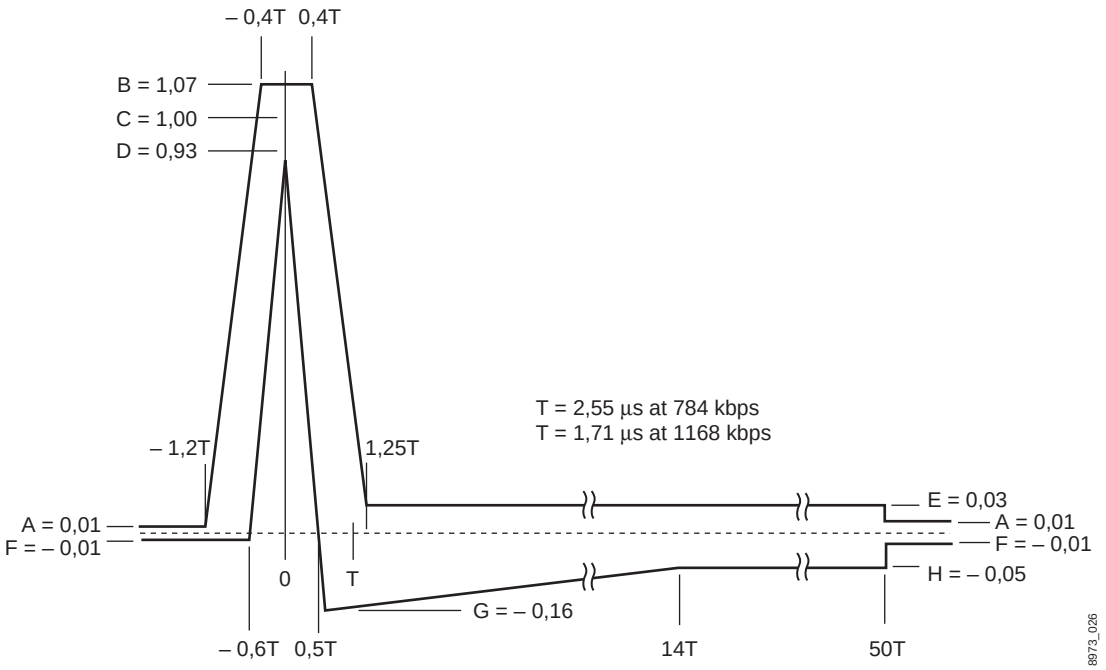


Table 5-19. Transmit Pulse Template for Two- and Three-Pair Systems (Source ETSI TS 101 135 Formerly ETR 152)

Normalized Level		Quaternary Symbols			
		+ 3	**+ 1**	**– 1**	**– 3**
A	0.01	0.0264	0.0088	–0.0088	–0.0264
B	1.07	2.8248	0.9416	–0.9416	–2.8248
C	1.00	2.6400	0.8800	–0.8800	–2.6400
D	0.93	2.4552	0.8184	–0.8184	–2.4552
E	0.03	0.0792	0.0264	–0.0264	–0.0792
F	–0.01	–0.0264	–0.0088	0.0088	0.0264
G	–0.16	–0.4224	–0.1408	0.1408	0.4224
H	–0.05	–0.1320	–0.0440	0.0440	0.1320

Figure 5-14. Transmit Pulse Template for One-Pair Systems (Source ETSI TS 101 135 Formerly ETR 152)

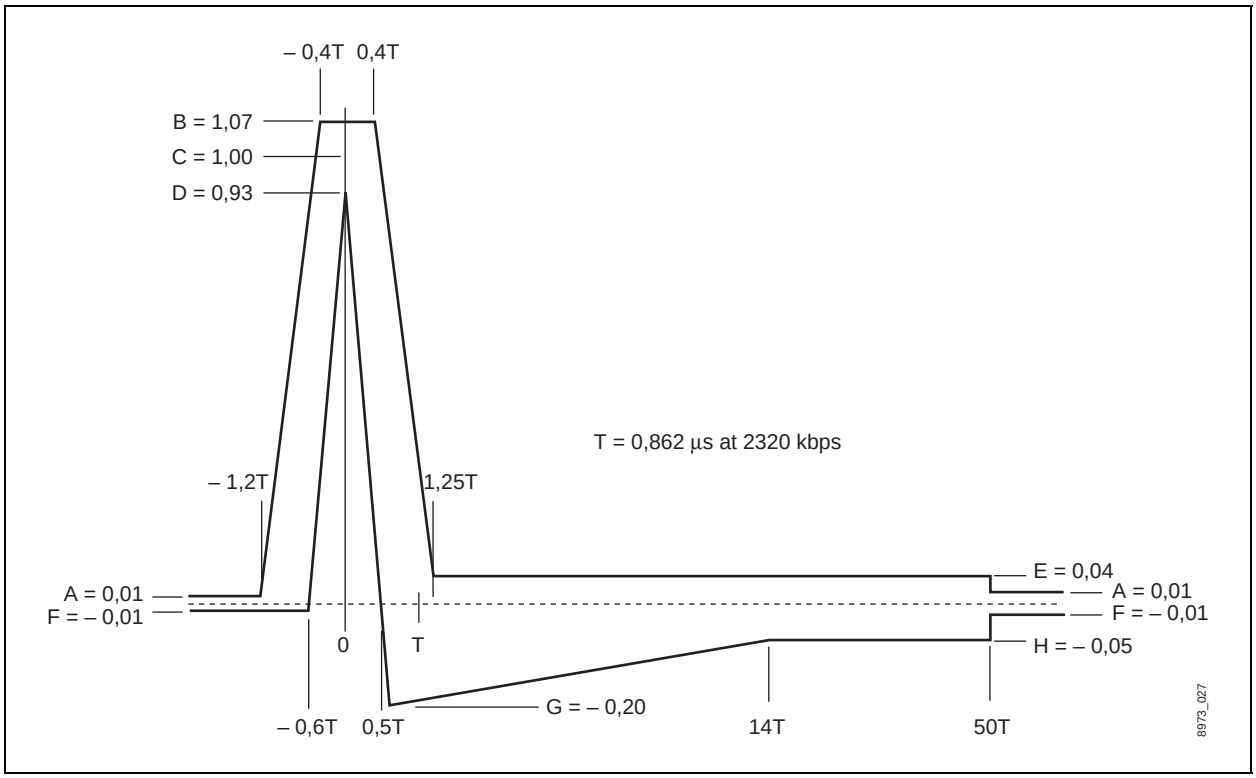


Table 5-20. Transmit Pulse Template for One-Pair Systems (Source ETSI TS 101 135 Formerly ETR 152)

Normalized Level		Quaternary Symbols			
		+ 3	**+ 1**	**– 1**	**– 3**
A	0.01	0.0250 V	0.0083 V	–0.0083 V	–0.0250 V
B	1.07	2.6750 V	0.8917 V	–0.8917 V	–2.6750 V
C	1.00	2.500 V	0.8333 V	–0.8333 V	–2.5000 V
D	0.93	2.3250 V	0.7750 V	–0.7750 V	–2.3250 V
E	0.04	0.1000 V	0.0333 V	–0.0333 V	–0.1000 V
F	–0.01	–0.0250 V	–0.0083 V	0.0083 V	0.0250 V
G	–0.20	–0.5000 V	–0.1667 V	0.1667 V	0.5000 V
H	–0.05	–0.1250 V	–0.0417 V	0.0417 V	0.1250 V

Figure 5-15. Upper Bound of the Average PSD of a 392 kbaud System (Source ETSI TS 101 135 Formerly ETR 152)

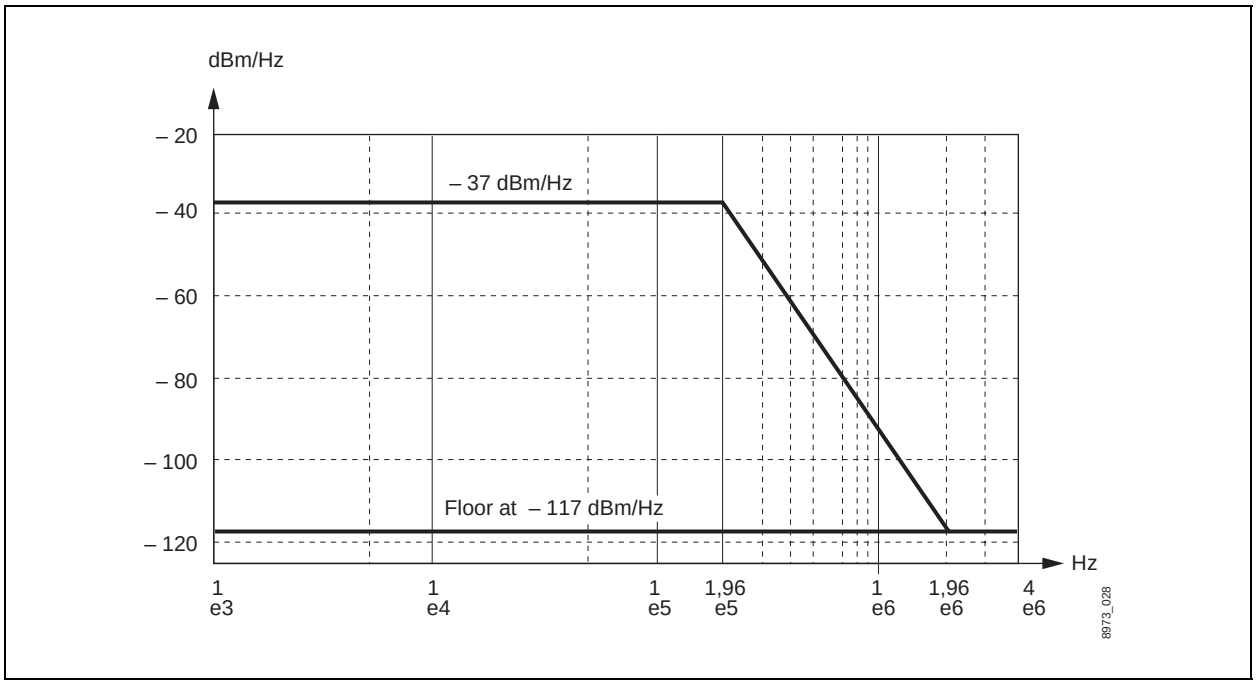


Figure 5-16. Upper Bound of the Average PSD of a 584 kbaud System (Source ETSI TS 101 135 Formerly ETR 152)

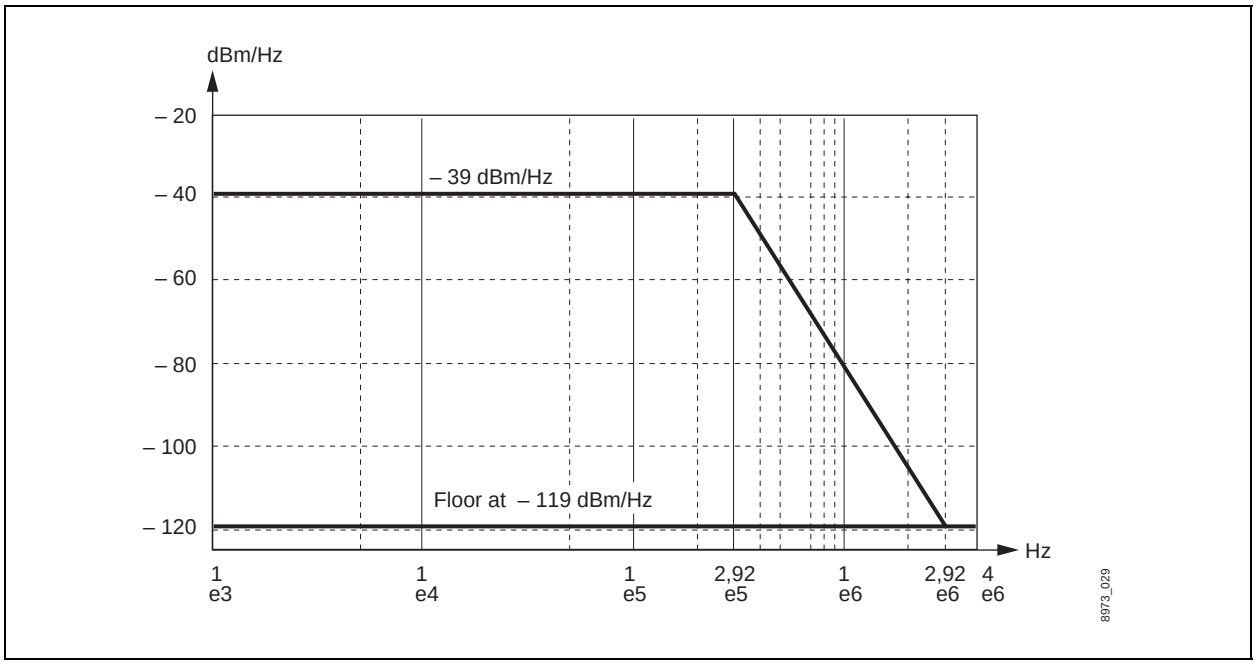
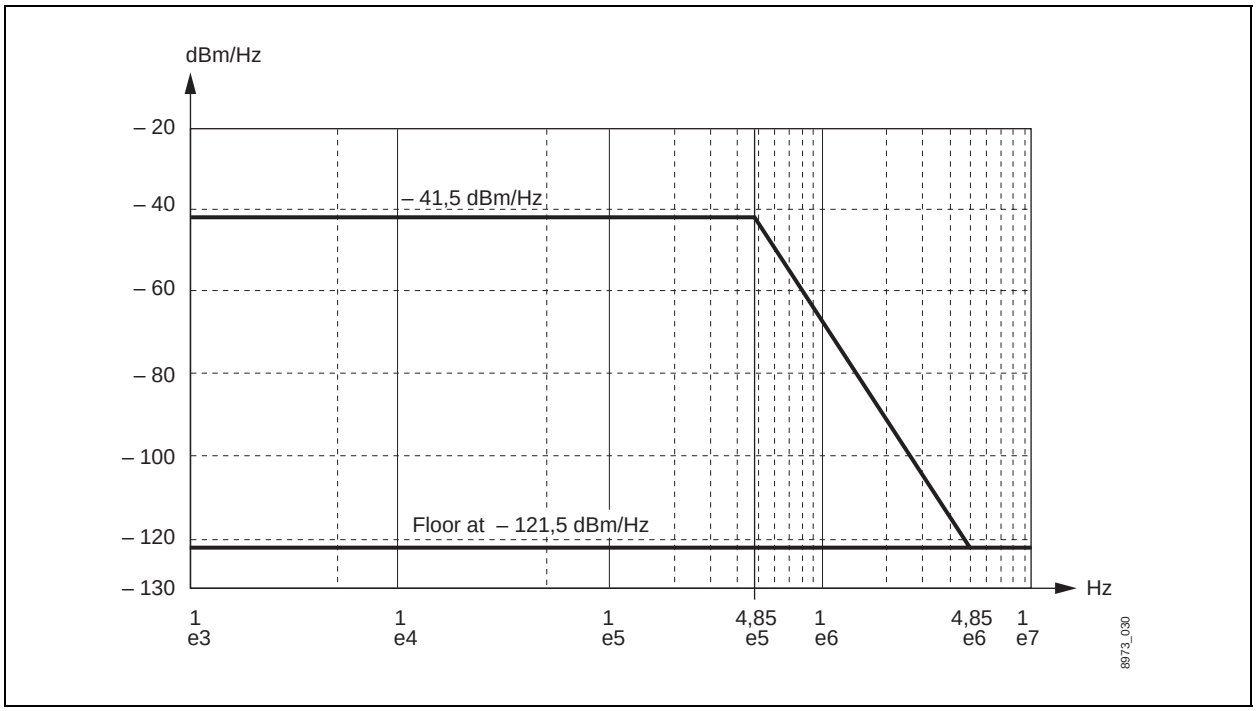


Figure 5-17. Upper Bound of the Average PSD of a 1160 kbaud System (Source ETSI TS 101 135 Formerly ETR 152)



5.9 Test Conditions

Figure 5-18 shows the transmitter test circuit. Figures 5-19 and 5-20 show the standard output and open-drain output loads, respectively.

Figure 5-18. Transmitter Test Circuit

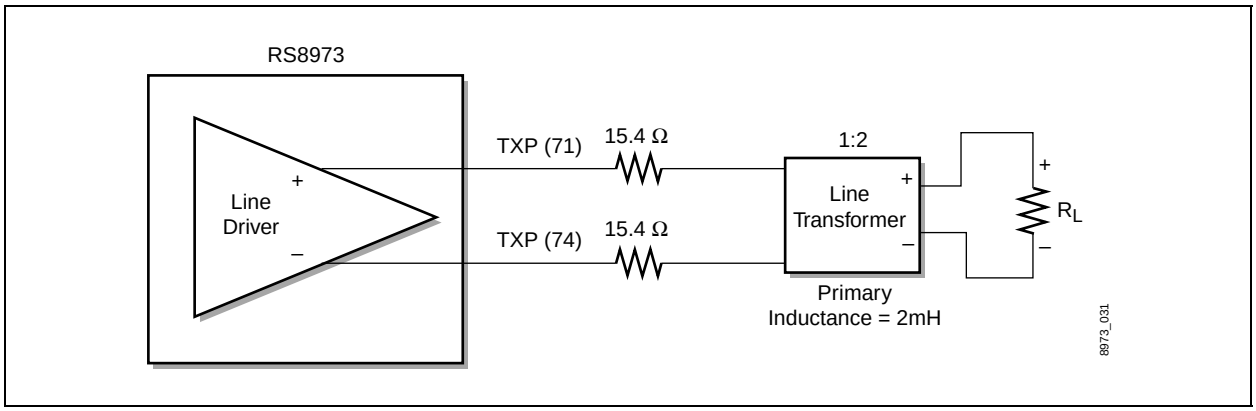


Figure 5-19. Standard Output Load (Totem Pole and Three-State Outputs)

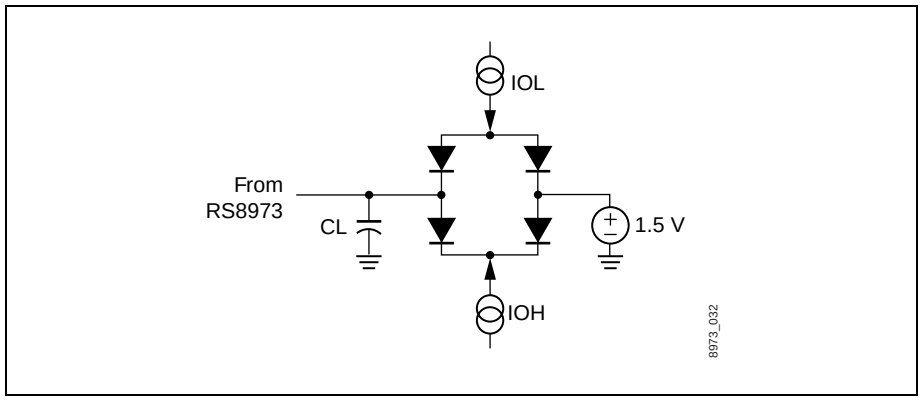
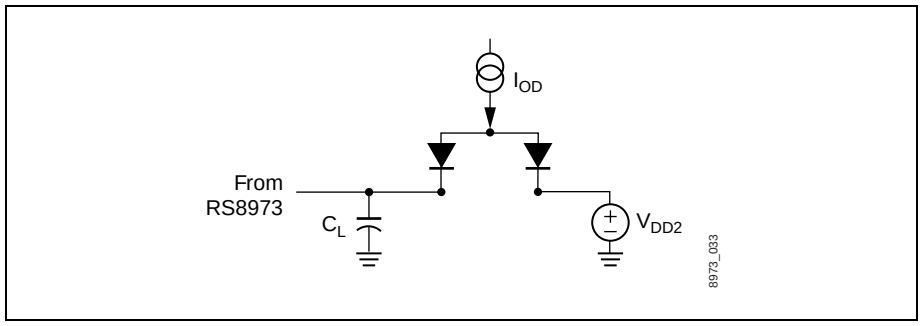


Figure 5-20. Open-Drain Output Load ($\overline{IRQ}$)



5.10 Timing Measurements

Figure 5-21 shows the input waveforms. Figures 5-22 and 5-23 show the output waveforms.

Figure 5-21. Input Waveforms for Timing Tests

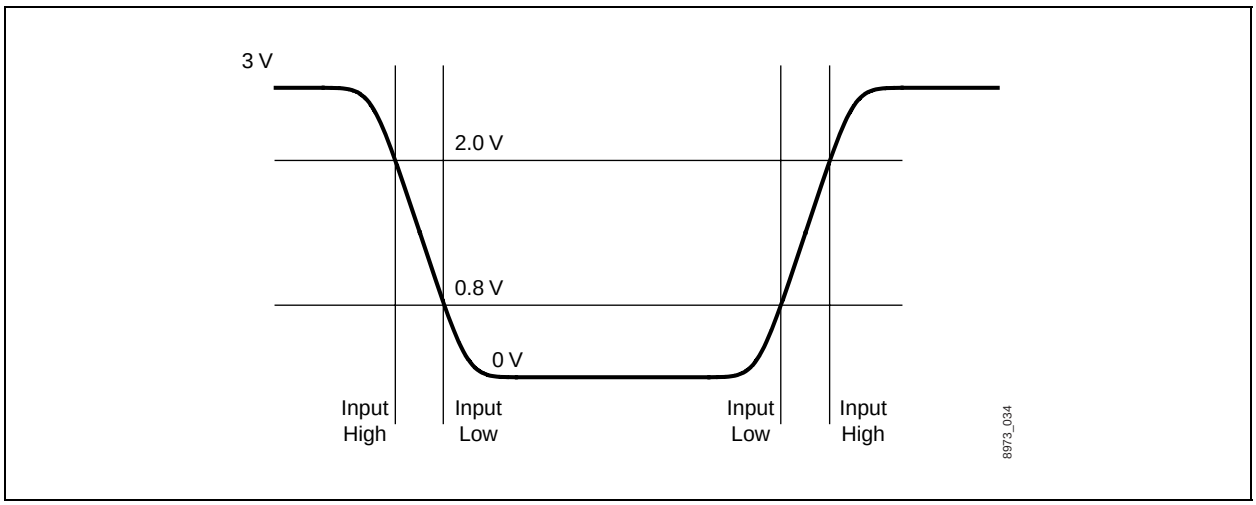


Figure 5-22. Output Waveforms for Timing Tests

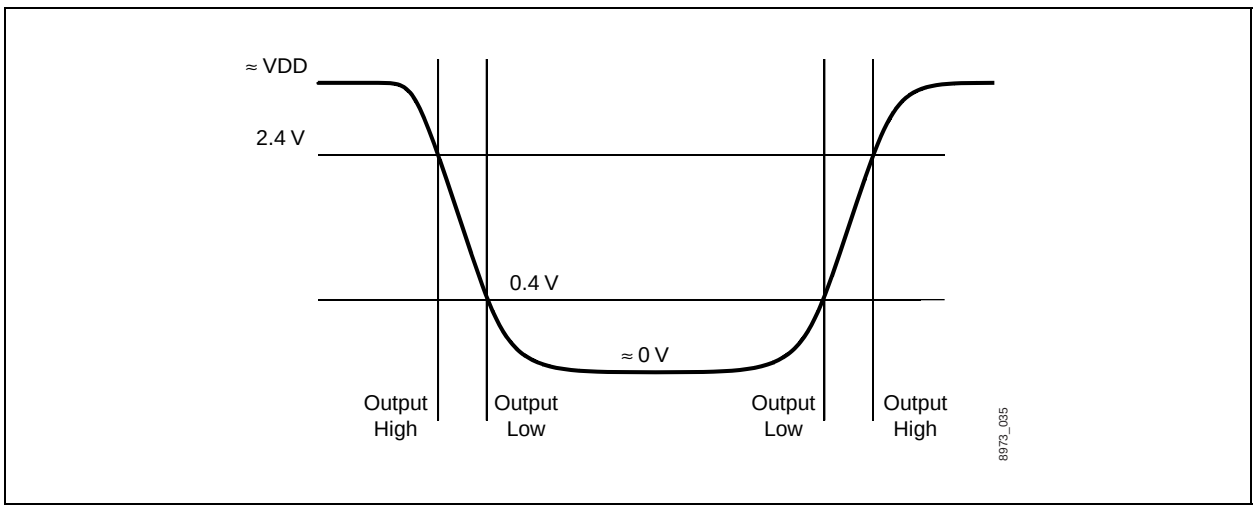
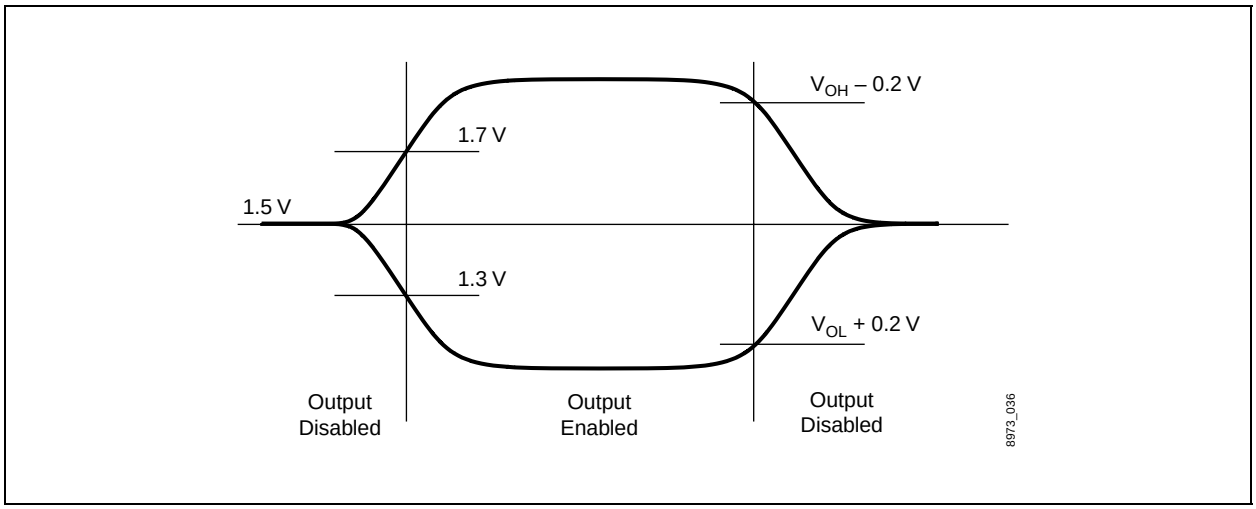
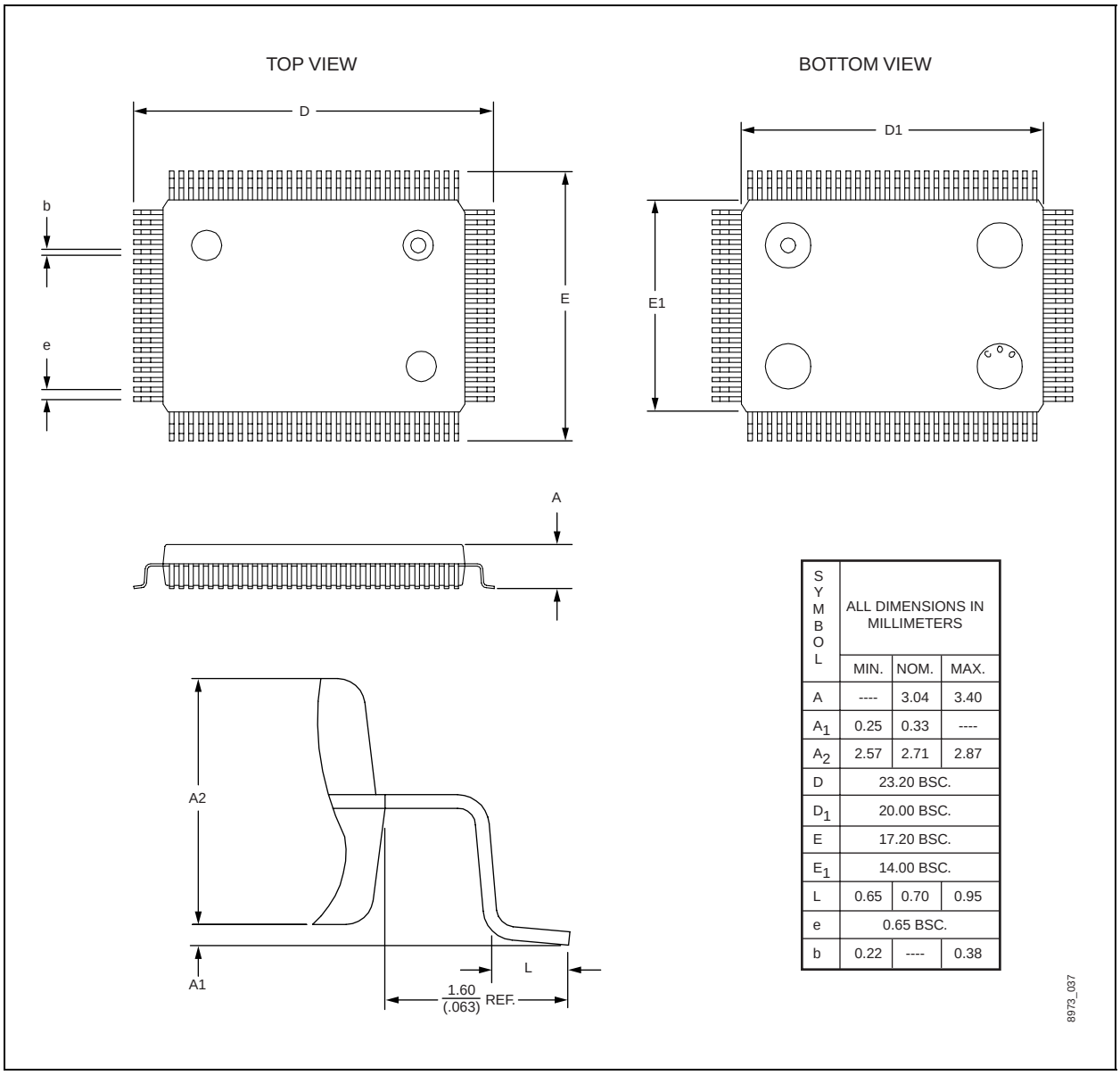


Figure 5-23. Output Waveforms for Three-state Enable and Disable Tests



5.11 Mechanical Specifications

Figure 5-24. 100-Pin PQFP



SYMBOL	ALL DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	----	3.04	3.40
A_1	0.25	0.33	----
A_2	2.57	2.71	2.87
D	23.20 BSC.		
D_1	20.00 BSC.		
E	17.20 BSC.		
E_1	14.00 BSC.		
L	0.65	0.70	0.95
e	0.65 BSC.		
b	0.22	----	0.38

Appendix A: Acronym List

The following list of acronyms and abbreviations does not include all signal, register, and bit names.

A	
ADC	analog-to-digital converter
AGC	automatic gain control
B	
BDSL	Boundary Scan Description Language
BER	bit error rate
2B1Q	Two binary, one quaternary encoding/decoding scheme
C	
COT	central office terminal
CT	continuous time
D	
DAC	digital-to-analog converter
DAGC	digital automatic gain control
DFE	decision feedback equalizer
DSP	digital signal processor
E	
EC	echo canceller
EP	error predictor
ETSI	European Telecommunications Standard Institute
F	
FELM	Far-end Level Meter
FFE	feed forward equalizer
FIR	finite impulse response
H	
HDSL	High-bit-rate Digital Subscriber Line
I	
IC	integrated circuit
IS	impulse shortening

J	
JTAG	Joint Test Action Group
L	
LEC	Linear Echo Canceller
LMS	least mean square
LSB	least significant bit
M	
MCI	microcomputer interface
MSB	most significant bit
N	
NEC	nonlinear echo canceller
P	
PCB	printed circuit board
PKD	Peak Detector
PLL	phase lock loop
PQFP	plastic quad flat pack
PSD	power spectral density
Q	
quat	quaternary
R	
RT	remote terminal
S	
SDSL	Symmetric Digital Subscriber Line over Single Pair
SLM	Signal Level Meter
SMON	serial monitor
SNR	signal-to-noise ratio
T	
TAP	test access port
TCK	test clock
TMS	test mode select
V	
VGA	variable gain amplifier
X	
XO	crystal oscillator

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