



Is Now Part of



**ON Semiconductor®**

To learn more about ON Semiconductor, please visit our website at  
[www.onsemi.com](http://www.onsemi.com)

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## FDC6301N Dual N-Channel , Digital FET

### General Description

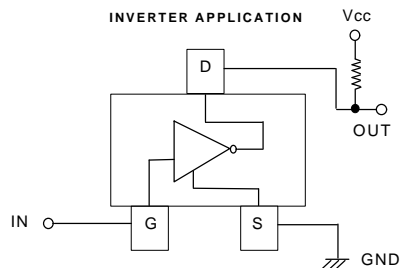
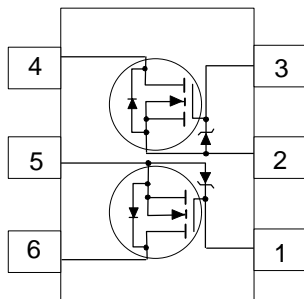
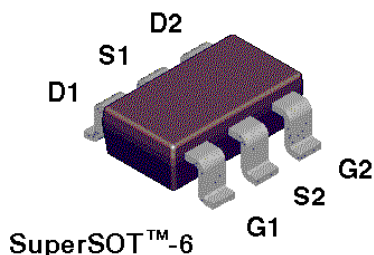
These dual N-Channel logic level enhancement mode field effect transistors are produced using Fairchild 's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for digital transistors. Since bias resistors are not required, these N-Channel FET's can replace several digital transistors, with a variety of bias resistors.

### Features

- 25 V, 0.22 A continuous, 0.5 A Peak.  
 $R_{DS(ON)} = 5 \Omega @ V_{GS} = 2.7 V$   
 $R_{DS(ON)} = 4 \Omega @ V_{GS} = 4.5 V.$
- Very low level gate drive requirements allowing direct operation in 3V circuits.  $V_{GS(th)} < 1.5V.$
- Gate-Source Zener for ESD ruggedness. >6kV Human Body Model.



Mark: .301



### Absolute Maximum Ratings $T_A = 25^\circ C$ unless other wise noted

Symbol	Parameter	FDC6301N	Units
$V_{DSS}, V_{CC}$	Drain-Source Voltage, Power Supply Voltage	25	V
$V_{GSS}, V_{IN}$	Gate-Source Voltage, $V_{IN}$	- 0.5 to +8	V
$I_D, I_{OUT}$	Drain/Output Current - Continuous - Pulsed	0.22	A
		0.5	
$P_D$	Maximum Power Dissipation (Note 1a) (Note 1b)	0.9	W
		0.7	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^\circ C$
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf / 1500 Ohm)	6.0	kV

### THERMAL CHARACTERISTICS

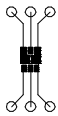
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	140	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	60	$^\circ C/W$

## Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	25			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		25		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
				$T_J = 55^\circ\text{C}$		10
$I_{GSS}$	Gate - Body Leakage Current	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$			100	nA
<b>ON CHARACTERISTICS (Note 2)</b>						
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-2.1		$\text{mV}/^\circ\text{C}$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.65	0.85	1.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 2.7\text{ V}, I_D = 0.2\text{ A}$		3.8	5	$\Omega$
				$T_J = 125^\circ\text{C}$	6.3	9
		$V_{GS} = 4.5\text{ V}, I_D = 0.4\text{ A}$		3.1	4	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 2.7\text{ V}, V_{DS} = 5\text{ V}$	0.2			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 0.4\text{ A}$		0.25		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		9.5		pF
$C_{oss}$	Output Capacitance			6		pF
$C_{rss}$	Reverse Transfer Capacitance			1.3		pF
<b>SWITCHING CHARACTERISTICS (Note 2)</b>						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 6\text{ V}, I_D = 0.5\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 50\ \Omega$		5	10	ns
$t_r$	Turn - On Rise Time			4.5	10	ns
$t_{D(off)}$	Turn - Off Delay Time			4	8	ns
$t_f$	Turn - Off Fall Time			3.2	7	ns
$Q_g$	Total Gate Charge	$V_{DS} = 5\text{ V}, I_D = 0.2\text{ A},$ $V_{GS} = 4.5\text{ V}$		0.49	0.7	nC
$Q_{gs}$	Gate-Source Charge			0.22		nC
$Q_{gd}$	Gate-Drain Charge			0.07		nC
<b>Inverter Electrical Characteristics (<math>T_A = 25^\circ\text{C}</math> unless otherwise noted)</b>						
$I_{O(off)}$	Zero Input Voltage Output Current	$V_{CC} = 20\text{ V}, V_I = 0\text{ V}$			1	$\mu\text{A}$
$V_{I(off)}$	Input Voltage	$V_{CC} = 5\text{ V}, I_O = 10\ \mu\text{A}$			0.5	V
$V_{I(on)}$		$V_O = 0.3\text{ V}, I_O = 0.005\text{ A}$	1			V
$R_{O(on)}$	Output to Ground Resistance	$V_I = 2.7\text{ V}, I_O = 0.2\text{ A}$		3.8	5	$\Omega$

**Notes:**

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.  $R_{\theta JA}$  shown below for single device operation on FR-4 in still air.



a.  $140^\circ\text{C}/\text{W}$  on a  $0.125\text{ in}^2$  pad of 2oz copper.



b.  $180^\circ\text{C}/\text{W}$  on a  $0.005\text{ in}^2$  pad of 2oz copper.

- Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

## Typical Electrical Characteristics

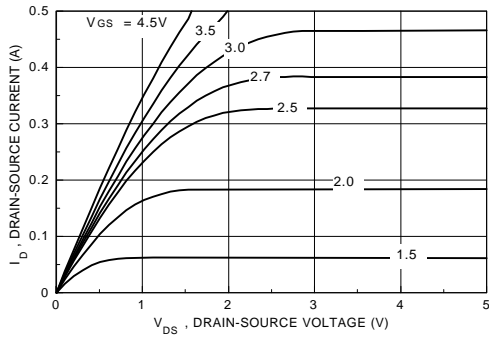


Figure 1. On-Region Characteristics.

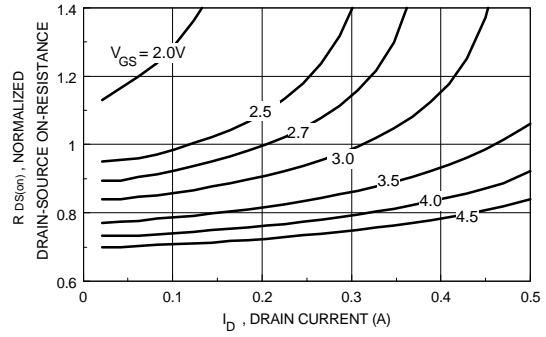


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

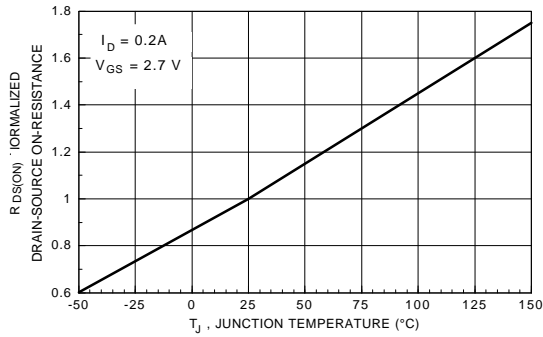


Figure 3. On-Resistance Variation with Temperature.

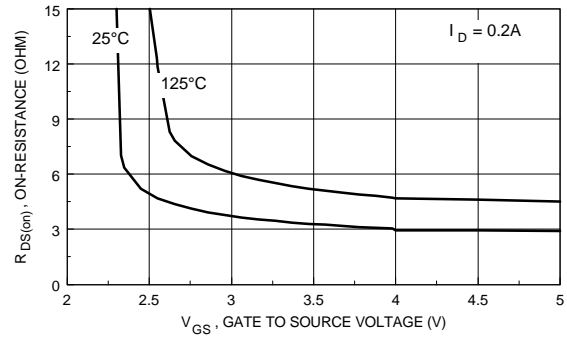


Figure 4. On Resistance Variation with Gate-To-Source Voltage.

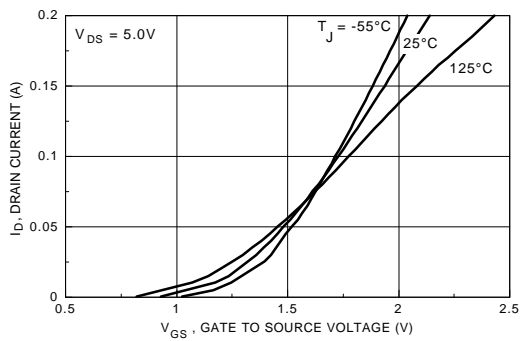


Figure 5. Transfer Characteristics.

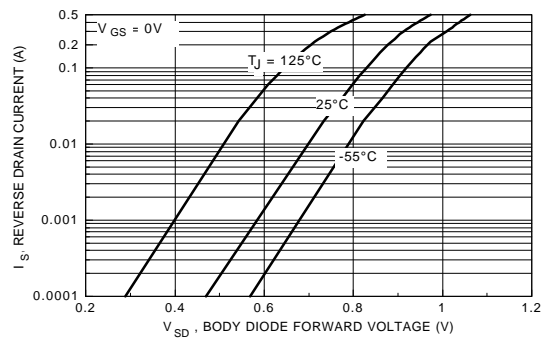


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Electrical Characteristics (continued)

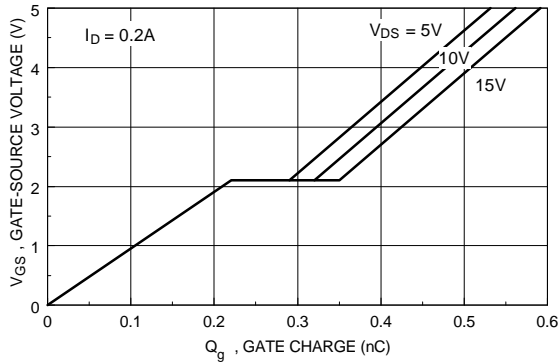


Figure 7. Gate Charge Characteristics.

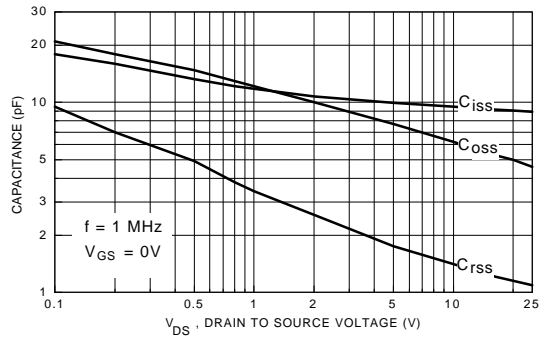


Figure 8. Capacitance Characteristics.

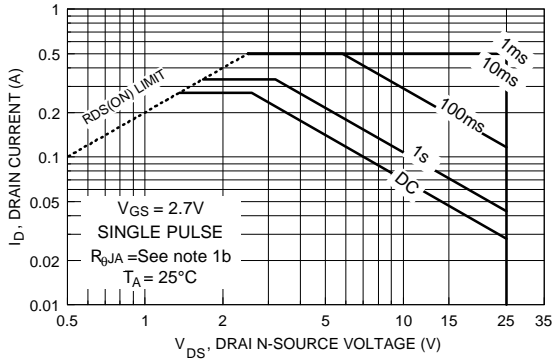


Figure 9. Maximum Safe Operating Area.

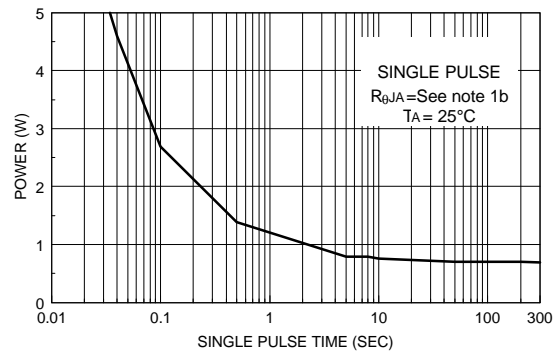


Figure 10. Single Pulse Maximum Power Dissipation.

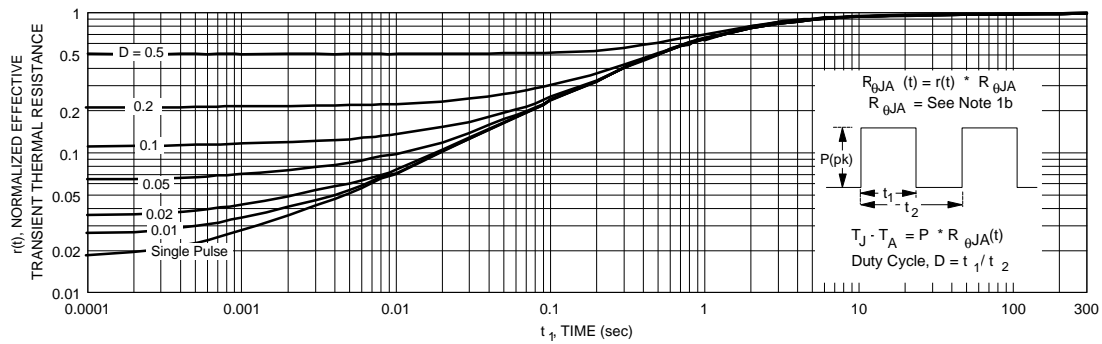


Figure 11. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1b. Transient thermal response will change depending on the circuit board design.

## TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE <sub>x</sub> <sup>™</sup>	FAST <sup>®</sup>	MICROWIRE <sup>™</sup>	SILENT SWITCHER <sup>®</sup>	UHC <sup>™</sup>
Bottomless <sup>™</sup>	FAST <sub>r</sub> <sup>™</sup>	OPTOLOGIC <sup>®</sup>	SMART START <sup>™</sup>	UltraFET <sup>®</sup>
CoolFET <sup>™</sup>	FRFET <sup>™</sup>	OPTOPLANAR <sup>™</sup>	SPM <sup>™</sup>	VCX <sup>™</sup>
CROSSVOLT <sup>™</sup>	GlobalOptoisolator <sup>™</sup>	PACMAN <sup>™</sup>	STAR*POWER <sup>™</sup>	
DenseTrench <sup>™</sup>	GTO <sup>™</sup>	POP <sup>™</sup>	Stealth <sup>™</sup>	
DOME <sup>™</sup>	HiSeC <sup>™</sup>	Power247 <sup>™</sup>	SuperSOT <sup>™</sup> -3	
EcoSPARK <sup>™</sup>	I <sup>2</sup> C <sup>™</sup>	PowerTrench <sup>®</sup>	SuperSOT <sup>™</sup> -6	
E <sup>2</sup> CMOS <sup>™</sup>	ISOPLANAR <sup>™</sup>	QFET <sup>™</sup>	SuperSOT <sup>™</sup> -8	
EnSigna <sup>™</sup>	LittleFET <sup>™</sup>	QS <sup>™</sup>	SyncFET <sup>™</sup>	
FACT <sup>™</sup>	MicroFET <sup>™</sup>	QT Optoelectronics <sup>™</sup>	TinyLogic <sup>™</sup>	
FACT Quiet Series <sup>™</sup>	MicroPak <sup>™</sup>	Quiet Series <sup>™</sup>	TruTranslation <sup>™</sup>	

STAR\*POWER is used under license

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.