MC54/74HC4538

Dual Precision Monostable Multivibrator (Retriggerable, Resettable)
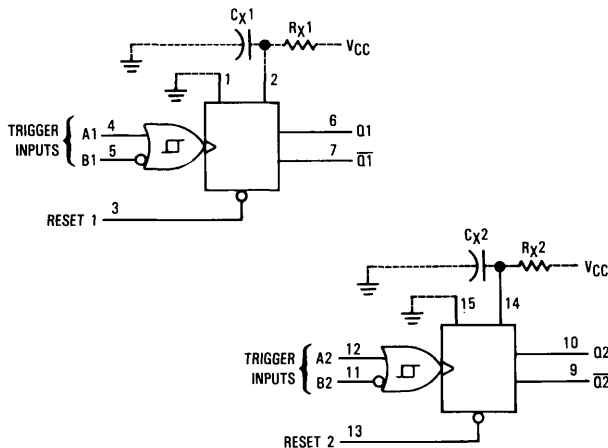## High-Performance Silicon-Gate CMOS

The MC54/74HC4538 is identical in pinout to the MC14538B and the MC14528B. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This dual monostable multivibrator may be triggered by either the positive or the negative edge of an input pulse, and produces a precision output pulse over a wide range of pulse widths. Because the device has conditioned trigger inputs, there are no trigger-input rise and fall time restrictions. The output pulse width is determined by the external timing components, R_X and C_X. The device has a reset function which forces the Q output low and the $\overline{Q}$ output high, regardless of the state of the output pulse circuitry.

- Unlimited Rise and Fall Times Allowed on the Trigger Inputs
- Output Pulse Width is Independent of the Trigger Pulse Width
- ±10% Guaranteed Pulse Width Variation from Part to Part (Using the Same Test Jig)
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 145 FETs or 36 Equivalent Gates

J SUFFIX
CERAMIC
CASE 620-09

N SUFFIX
PLASTIC
CASE 648-08

ORDERING INFORMATION

MC74HCXXXXN	Plastic
MC54HCXXXXJ	Ceramic

$T_A = -55°$ to 125°C for all packages.
Dimensions in Chapter 6.

PIN ASSIGNMENT

GND	1 ●	16	V_{CC}
C_X1/R_X1	2	15	GND
RESET 1	3	14	C_X2/R_X2
A1	4	13	RESET 2
B1	5	12	A2
Q1	6	11	B2
$\overline{Q1}$	7	10	Q2
GND	8	9	$\overline{Q2}$

LOGIC DIAGRAM

PIN 16 = V_{CC}
PIN 8 = GND
R_X AND C_X ARE EXTERNAL COMPONENTS
PIN 1 AND PIN 15 MUST BE HARD WIRED TO GND

FUNCTION TABLE

Inputs			Outputs	
Reset	A	B	Q	$\overline{Q}$
H	⤒	H	⊓	⊔
H	L	⤓	⊓	⊔
H	X	L	Not Triggered	
H	H	X	Not Triggered	
H	L,H,⤓	H	Not Triggered	
H	L	L,H,⤒	Not Triggered	
L	X	X	L	H
⤓⤒	X	X	Not Triggered	

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to $+7.0$	V
V_{in}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin—A, B, Reset	± 20	mA
I_{in}	DC Input Current, per Pin—C_X/R_X	± 30	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
T_{stg}	Storage Temperature	-65 to $+150$	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	 260 300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
 Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C
          Ceramic DIP: -10 mW/°C from 100° to 125°C
For high frequency or heavy load considerations, see Chapter 4.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-55	$+125$	°C
t_r, t_f	Input Rise and Fall Time—Reset (Figure 5)	$V_{CC} = 2.0$ V $V_{CC} = 4.5$ V $V_{CC} = 6.0$ V	0 0 0	1000 500 400	ns
	A or B (Figure 5)		—	no limit	
R_X	External Timing Resistor	$V_{CC} < 4.5$ V $V_{CC} \geq 4.5$ V	10 2.0	* *	kΩ
C_X	External Timing Capacitor		0	*	μF

*The maximum allowable values of R_X and C_X are a function of the leakage of capacitor C_X, the leakage of the HC4538, and leakage due to board layout and surface resistance. For most applications, C_X/R_X should be limited to a maximum value of 10 μF/1 MΩ. Values of $C_X > 1.0$ μF may cause a problem during power down (see Power-Down Considerations). Susceptibility to externally induced noise signals may occur for $R_X > 1$ MΩ.

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to −55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $\|I_{out}\| \leq 20\ \mu A$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1$ V or $V_{CC} - 0.1$ V $\|I_{out}\| \leq 20\ \mu A$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 20\ \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.70 5.20	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 20\ \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.40 0.40	
I_{in}	Maximum Input Leakage Current (A, B, Reset)	$V_{in} = V_{CC}$ or GND	6.0	±0.1	±1.0	±1.0	μA
I_{in}	Maximum Input Leakage Current (C_X/R_X)	$V_{in} = V_{CC}$ or GND	6.0	±50	±500	±500	nA
I_{CC}	Maximum Quiescent Supply Current (per Package) Standby State	$V_{in} = V_{CC}$ or GND Q1 and Q2 = Low $I_{out} = 0\ \mu A$	6.0	130	220	350	μA
I_{CC}	Maximum Supply Current (per Package) Active State	$V_{in} = V_{CC}$ or GND Q1 and Q2 = High $I_{out} = 0\ \mu A$ Pins 2 and 14 = 0.5 V_{CC}	6.0	150	250	400	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{PLH}	Maximum Propagation Delay, Input A or B to Q (Figures 4 and 6)	2.0 4.5 6.0	250 50 43	315 63 54	375 75 64	ns
t_{PHL}	Maximum Propagation Delay, Input A or B to $\overline{Q}$ (Figures 4 and 6)	2.0 4.5 6.0	275 55 47	345 69 59	415 83 71	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q (Figures 5 and 6)	2.0 4.5 6.0	250 50 43	315 63 54	375 75 64	ns
t_{PLH}	Maximum Propagation Delay, Reset to $\overline{Q}$ (Figures 5 and 6)	2.0 4.5 6.0	275 55 47	345 69 59	415 83 71	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 5 and 6)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance (A, B, Reset) (C_X, R_X)	− −	10 25	10 25	10 25	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Multivibrator) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	**Typical @ 25°C, $V_{CC} = 5.0$ V**	
		150	pF

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TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{rec}	Minimum Recovery Time, Reset Inactive to A or B (Figure 5)	2.0 4.5 6.0	0 0 0	0 0 0	0 0 0	ns
t_W	Minimum Pulse Width, Input A or B (Figure 4)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_W	Minimum Pulse Width, Reset (Figure 5)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times, Reset (Figure 5)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns
	A or B (Figure 5)	2.0 4.5 6.0	No Limit			

NOTE: Information on typical parametric values can be found in Chapter 4.

OUTPUT PULSE WIDTH CHARACTERISTICS ($C_L = 50$ pF)

Symbol	Parameter	Conditions		Temperature						Unit
		Timing Components	V_{CC} V	25°C		−40° to 85°C		−55° to 125°C		
				Min	Max	Min	Max	Min	Max	
τ	Output Pulse Width* (Figures 4 and 6)	$R_X = 10$ kΩ, $C_X = 0.1$ μF	5.0	0.63	0.77	0.60	0.80	0.59	0.81	ms
—	Pulse Width Match Between Circuits in the Same Package	—	—	±5						%
—	Pulse Width Match Variation (Part to Part)	—	—	±10						%

*For output pulse widths greater than 100 μs, typically $\tau = k R_X C_X$, where the value of k may be found in Figure 1.
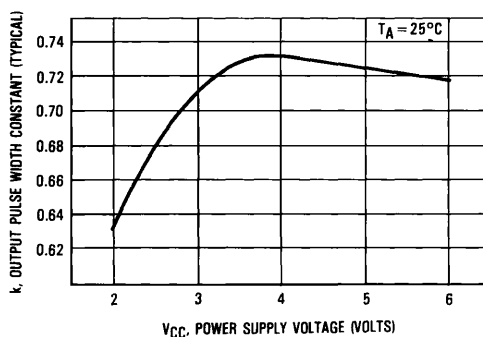
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Figure 1. Typical Output Pulse Width Constant, k, versus Supply Voltage
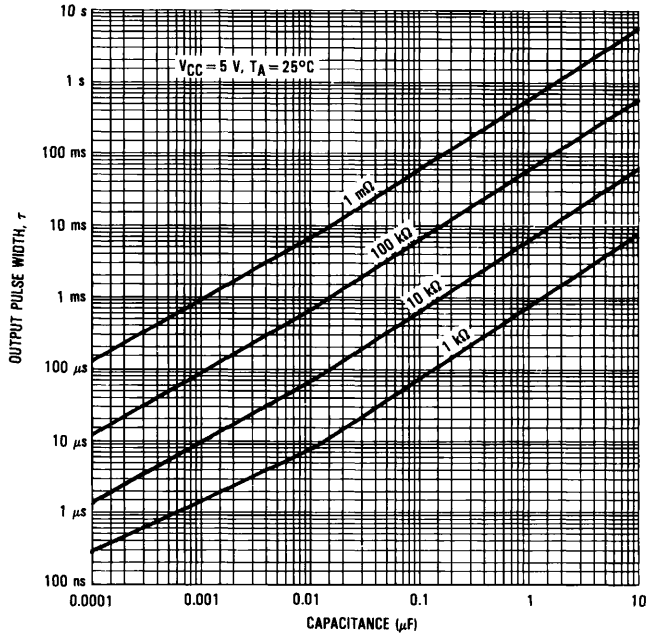(For output pulse widths ≥ 100 μs: $\tau = k R_X C_X$)

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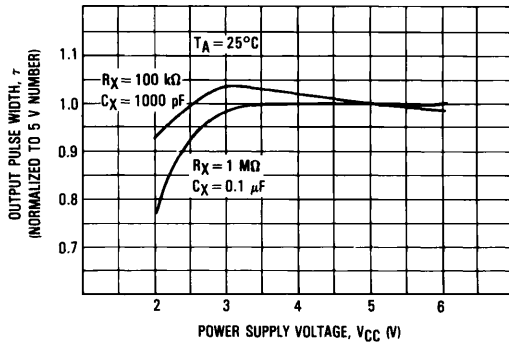Figure 2. Output Pulse Width vs. Timing Capacitance

Figure 3. Normalized Output Pulse Width
versus Power Supply Voltage

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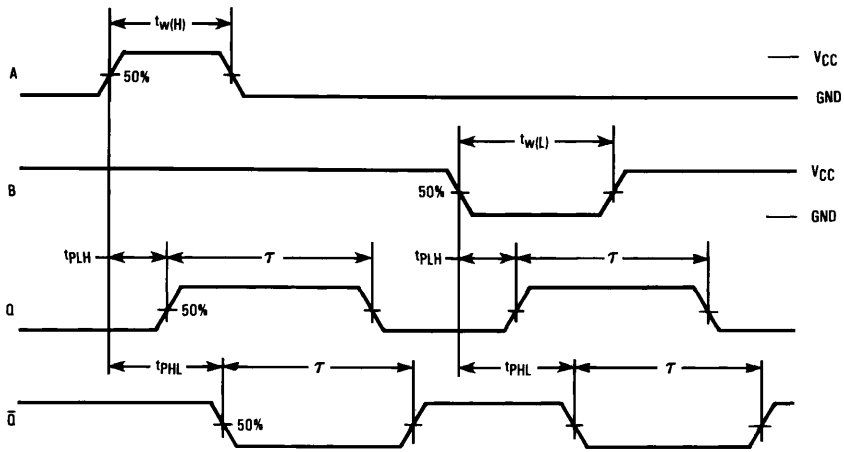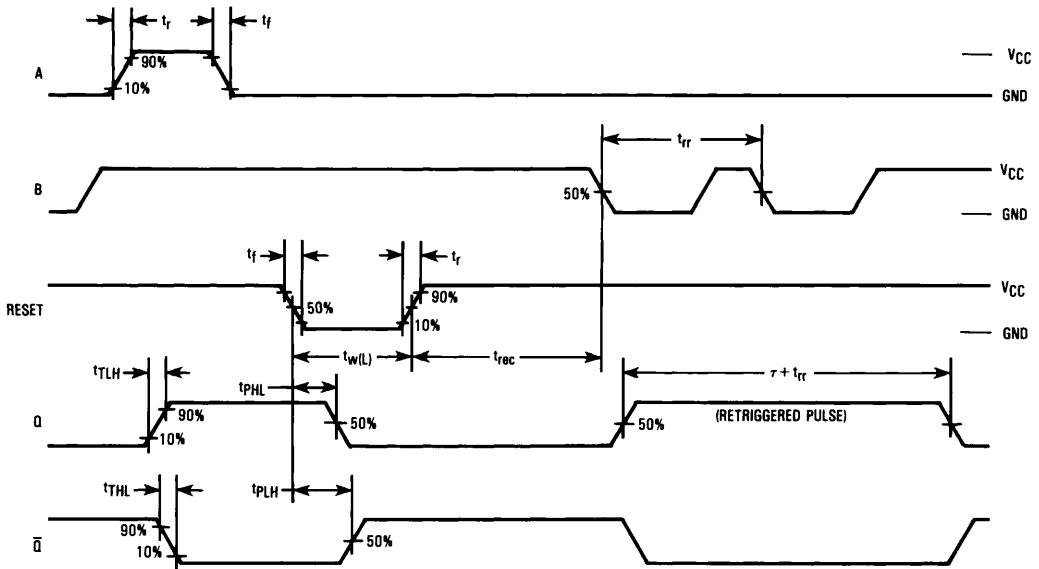# MC54/74HC4538

SWITCHING WAVEFORMS
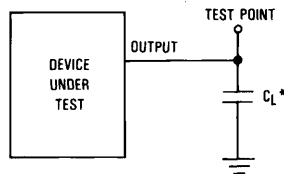

Figure 4

Figure 5

*Includes all probe and jig capacitance.

Figure 6. Test Circuit

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PIN DESCRIPTIONS

INPUTS

A1, A2 (PINS 4, 12) — Positive-edge trigger inputs. A rising-edge signal on either of these pins triggers the corresponding multivibrator when there is a high level on the B1 or B2 input.

B1, B2 (PINS 5, 11) — Negative-edge trigger inputs. A falling-edge signal on either of these pins triggers the corresponding multivibrator when there is a low level on the A1 or A2 input.

RESET 1, RESET 2 (PINS 3, 13) — Reset inputs (active low). When a low level is applied to one of these pins, the Q output of the corresponding multivibrator is reset to a low level and the $\overline{Q}$ output is set to a high level.

C_X1/R_X1 and C_X2/R_X2 (PINS 2 and 14) — External timing components. These pins are tied to the common points of the external timing resistors and capacitors (see the Block Diagram). Polystyrene capacitors are recommended for optimum pulse width control. Electrolytic capacitors are not recommended due to high leakages associated with these type capacitors.

GND (PINS 1 and 15) — External ground. The external timing capacitors discharge to ground through these pins.

OUTPUTS

Q1, Q2 (PINS 6, 10) — Noninverted monostable outputs. These pins (normally low) pulse high when the multivibrator is triggered at either the A or the B input. The width of the pulse is determined by the external timing components, R_X and C_X.

$\overline{Q1}$, $\overline{Q2}$ (PINS 7, 9) — Inverted monostable outputs. These pins (normally high) pulse low when the multivibrator is triggered at either the A or the B input. These outputs are the inverse of Q1 and Q2.
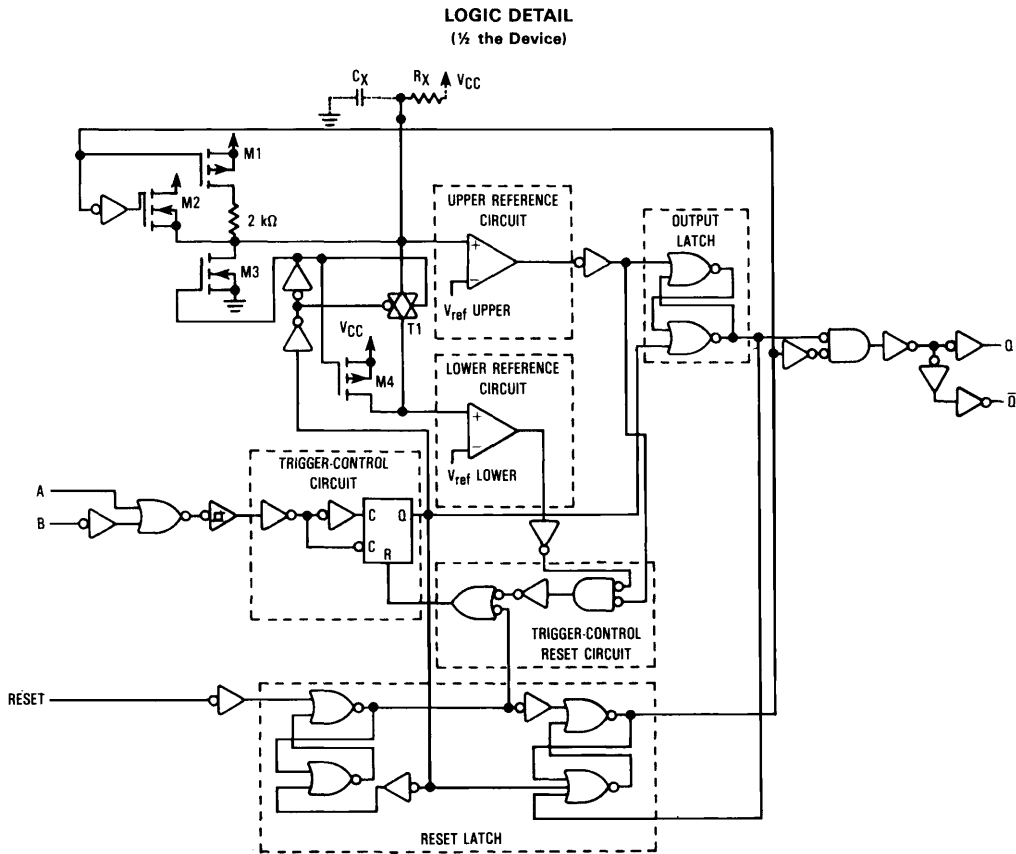
LOGIC DETAIL
(½ the Device)

Figure 7

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CIRCUIT OPERATION

Figure 10 shows the HC4538 configured in the retriggerable mode. Briefly, the device operates as follows (refer to Figure 7): In the quiescent state, the external timing capacitor, C_X, is charged to V_{CC}. When a trigger occurs, the Q output goes high and C_X discharges quickly to the lower reference voltage (V_{ref} Lower ≈ 1/3 V_{CC}). C_X then charges, through R_X, back up to the upper reference voltage (V_{ref} Upper ≈ 2/3 V_{CC}), at which point the one-shot has timed out and the Q output goes low.

The following, more detailed description of the circuit operation refers to both the logic detail (Figure 7) and the timing diagram (Figure 8).

QUIESCENT STATE

In the quiescent state, before an input trigger appears, the output latch is high and the reset latch is high (#1 in Figure 8). Thus the Q output (pin 6 or 10) of the monostable multivibrator is low (#2, Figure 8).

The output of the trigger-control circuit is low (#3), and transistors M1, M2, and M3 are turned off. The external timing capacitor, C_X, is charged to V_{CC} (#4), and the upper reference circuit has a low output (#5). Transistor M4 is turned on and

transmission gate T1 is turned off. Thus the lower reference circuit has V_{CC} at the noninverting input and a resulting low output (#6).

In addition, the output of the trigger-control reset circuit is low.

TRIGGER OPERATION

The HC4538 is triggered by either a rising-edge signal at input A (#7) or a falling-edge signal at input B (#8), with the unused trigger input and the Reset input held at the voltage levels shown in the Function Table. Either trigger signal will cause the output of the trigger-control circuit to go high (#9).

The trigger-control circuit going high simultaneously initiates three events. First, the output latch goes low, thus taking the Q output of the HC4538 to a high state (#10). Second, transistor M3 is turned on, which allows the external timing capacitor, C_X, to rapidly discharge toward ground (#11). (Note that the voltage across C_X appears at the input of the upper reference circuit comparator). Third, transistor M4 is turned off and transmission gate T1 is turned on, thus allowing the voltage across C_X to also appear at the input of the lower reference circuit comparator.
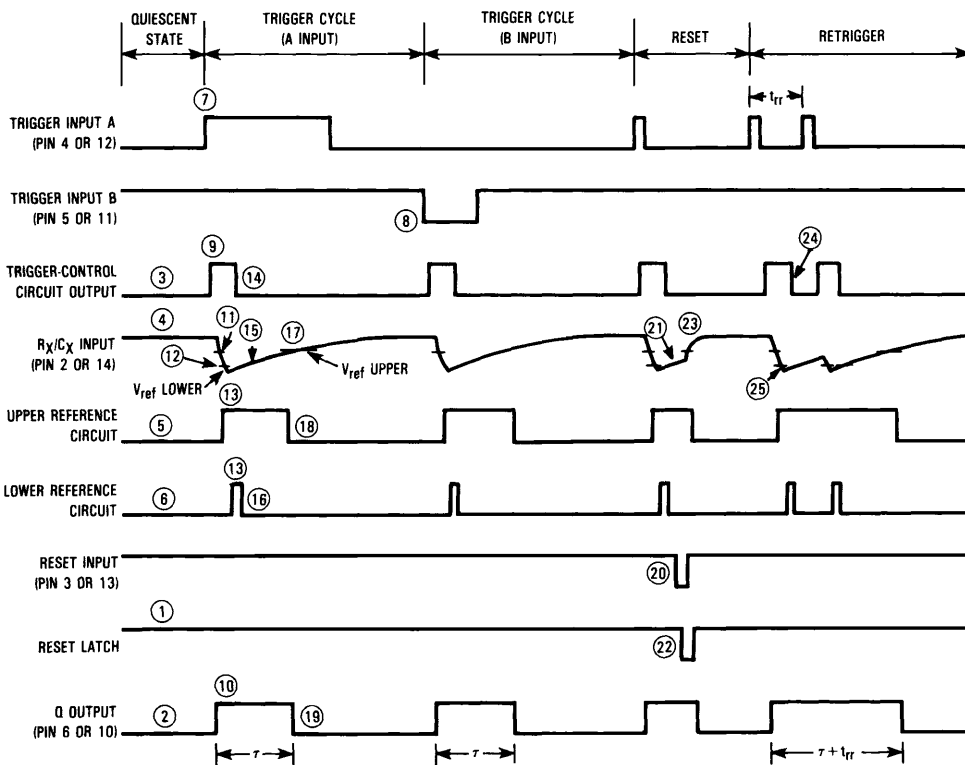

Figure 8. Timing Diagram

When C_X discharges to the reference voltage of the lower reference circuit (#12), the outputs of both reference circuits will be high (#13). The trigger-control reset circuit goes high, resetting the trigger-control circuit flip-flop to a low state (#14). This turns transistor M3 off again, allowing C_X to begin to charge back up toward V_{CC}, with a time constant $t = R_X C_X$ (#15). In addition, transistor M4 is turned on and transmission gate T1 is turned off. Thus a high voltage level is applied to the input of the lower reference circuit comparator, causing its output to go low (#16). The monostable multivibrator may be retriggered at any time after the trigger-control circuit goes low.

When C_X charges up to the reference voltage of the upper reference circuit (#17), the output of the upper reference circuit goes low (#18). This causes the output latch to toggle, taking the Q output of the HC4538 to a low state (#19), and completing the time-out cycle.

POWER-DOWN CONSIDERATIONS

Large values of C_X may cause problems when powering down the HC4538 because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from V_{CC} through the input protection diodes at pin 2 or pin 14. Current through the protection diodes must be limited to 30 mA; therefore, the turn-off time of the V_{CC} power supply must not be faster than $t = V_{CC} \cdot C_X / (30 \text{ mA})$. For example, if $V_{CC} = 5$ V and $C_X = 15 \ \mu F$, the V_{CC} supply must turn off no faster than $t = (5 \text{ V}) \cdot (15 \ \mu F) / 30 \text{ mA} = 2.5$ ms. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of V_{CC} to zero volts occurs, the HC4538 may sustain damage. To avoid this possibility, use an external damping diode, D_X, connected as shown in Figure 9. Best results can be achieved if diode D_X is chosen to be a germanium or Schottky type diode able to withstand large current surges.

RESET OPERATION

A low voltage applied to the Reset pin always forces the Q output of the HC4538 to a low state.

The timing diagram illustrates the case in which reset occurs (#20) while C_X is charging up toward the reference voltage of the upper reference circuit (#21). When a reset occurs, the output of the reset latch goes low (#22), turning on transistor M1. Thus C_X is allowed to quickly charge up to V_{CC} (#23) to await the next trigger signal.

RETRIGGER OPERATION

When used in the retriggerable mode (Figure 10), the HC4538 may be retriggered during timing out of the output pulse at any time after the trigger-control circuit flip-flop has been reset (#24). Because the trigger-control circuit flip-flop resets shortly after C_X has discharged to the reference voltage of the lower reference circuit (#25), the minimum retrigger time, t_{rr} (Figure 5) is a function of internal propagation delays and the discharge time of C_X.

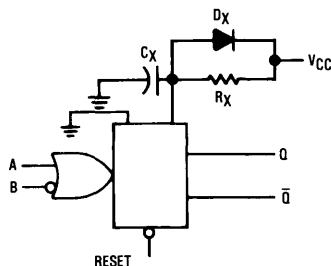Figure 11 shows the device configured in the nonretriggerable mode.

Figure 9. Discharge Protection During Power Down
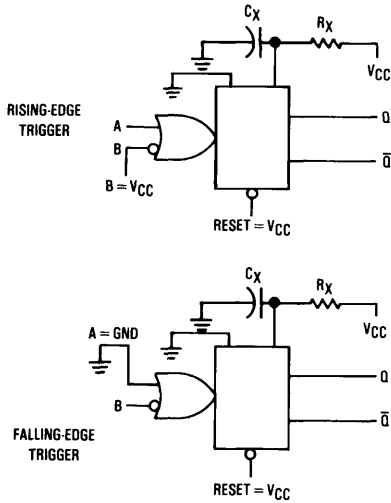
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TYPICAL APPLICATIONS

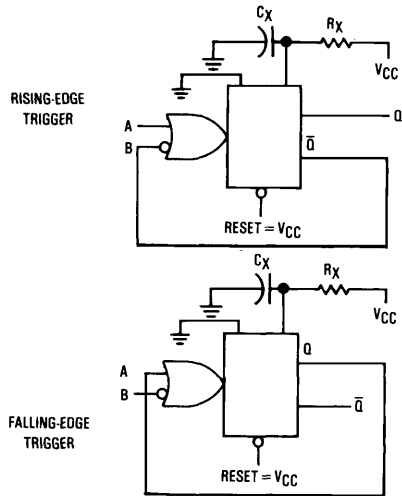**Figure 10. Retriggerable Monostable Circuitry**

Figure 11. Nonretriggerable Monostable Circuitry

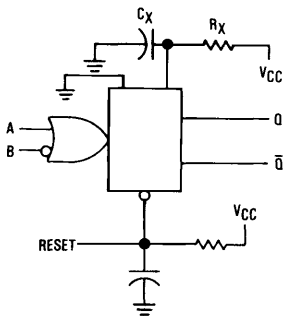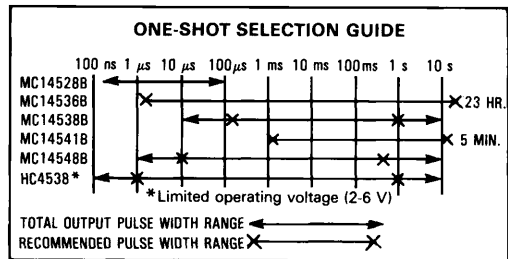**Figure 12. Elimination of Output Pulse Width During Power-Up**

ONE-SHOT SELECTION GUIDE

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