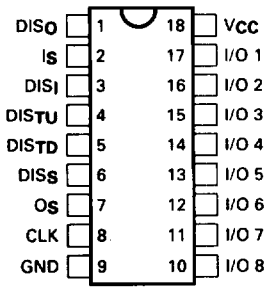
ADVANCE INFORMATION

DUAL RANK 8-BIT SHIFT REGISTERS WITH 3-STATE OUTPUTS

APRIL 1989

- **Serial-to-Parallel and Parallel-to Serial Conversion**
- **Data Exchangeable between I/O-Register and Shift Register**
- **Registers are edge-triggered by the positive transition of the clock**
- **All inputs are PNP transistors**
- **Input disable dominates over output disable**
- **3-state I/O buffers are designed for high speed bus-oriented systems**
- **24 mA output low current at I/O ports**
- **16 mA output low current at serial output**
- **Designed in ALS technology for low power consumption**
- **All control inputs are active low**
- **Device can be cascaded to N-bit word**

N PACKAGE
(TOP VIEW)



description

These circuits are 3-state, edge-triggered, 8-bit I/O registers in parallel with 8-bit serial shift registers which are capable of operating in any of the following modes:

parallel load from I/O pins to register 'A',

parallel transfer down from register 'A' to serial shift register 'B',

parallel transfer up from shift register 'B' to register 'A',

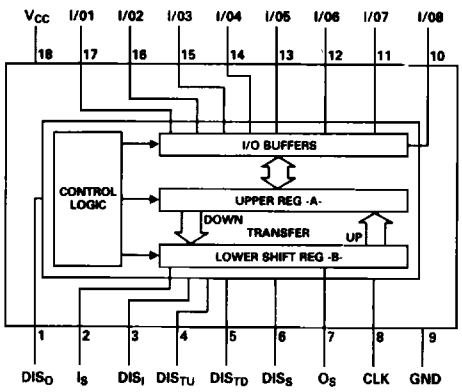
serial shift of register 'B' or exchange data between register 'A' and shift register 'B'.

Since the register are edge-triggered by the positive transition of the clock, the control lines which determine the mode or operation are completely independent of the logic level applied to the clock.

Designed for bus-oriented systems, these circuits have their 3-state inputs and outputs on the same pins.

logic symbol

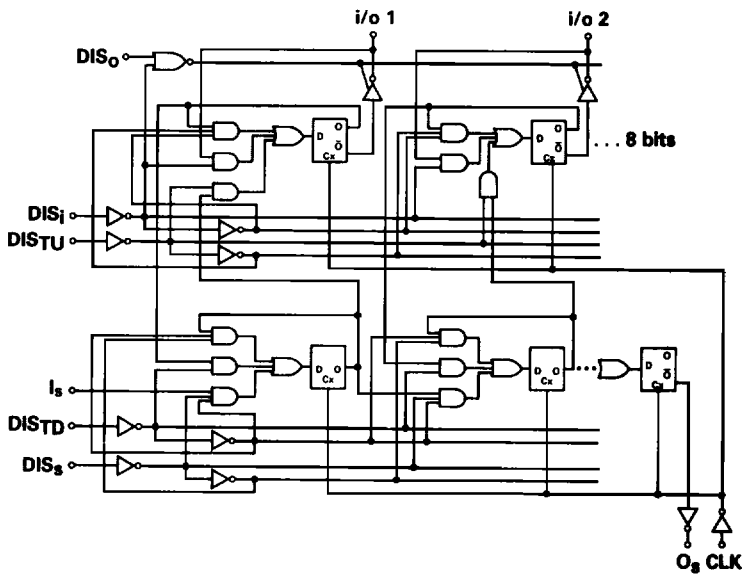
Dual-In-Line Package



Pin Description

DIS_O – Output disable
I_S – Serial input
DIS_I – Input disable
DIS_{TU} – Transfer up disable
DIS_{TD} – Transfer down disable
DIS_S – Shift disable
O_S – Serial output
CLK – Clock
GND – Ground
I/O 1 ... I/O 8 – 8-bit I/O pins
V_{CC} – Supply Voltage

logic diagram



TEXAS INSTRUMENTS

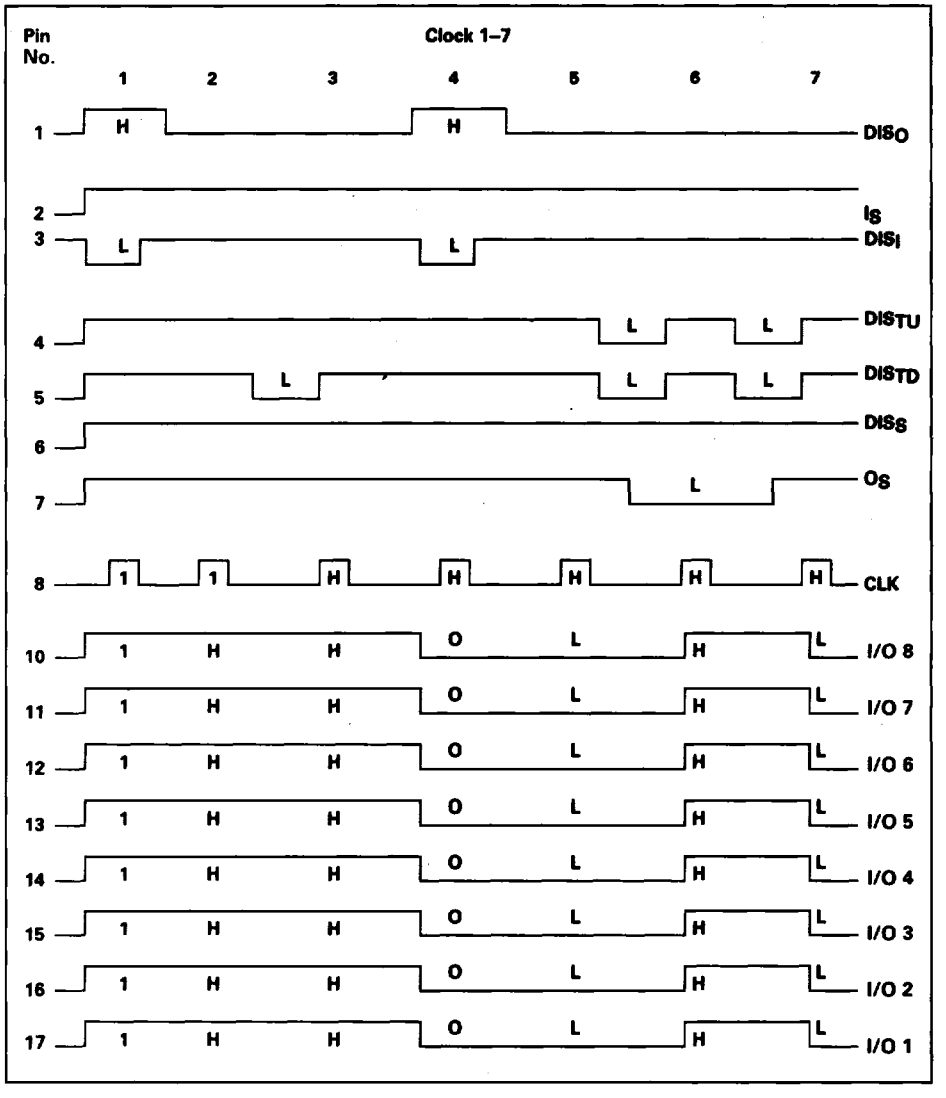
truth tables

TABLE I

	DIS O	DIS I	DIS TU	DIS TD	DIS S	CLK	IS	8-BIT I/O PINS	CONTENT OF UPPER REG. "A" A1 A2 A3 A4 A5 A6 A7 A8	CONTENT OF LOWER SERIAL SHIFT REG. "B" B1 B2 B3 B4 B5 B6 B7 B8	OS	COMMENTS
1	H	H	H	H	H	X	X	Hi-Z	a1 a2 a3 a4 a5 a6 a7 a8	b1 b2 b3 b4 b5 b6 b7 b8	b8	Stable state
2	L	H	H	H	H	X	X	Output	a1 a2 a3 a4 a5 a6 a7 a8	b1 b2 b3 b4 b5 b6 b7 b8	b8	Entering data from I/O
3	X	L	H	H	H	↑	X	Input	I1 I2 I3 I4 I5 I6 I7 I8	b1 b2 b3 b4 b5 b6 b7 b8	b8	to reg. "A"
4	H	H	L	H	H	↑	X	Hi-Z	b1 b2 b3 b4 b5 b6 b7 b8	b1 b2 b3 b4 b5 b6 b7 b8	b8	Transfer data up from
5	L	H	L	H	H	↑	X	Output	b1 b2 b3 b4 b5 b6 b7 b8	b1 b2 b3 b4 b5 b6 b7 b8	b8	reg. "B" to reg."A"
6	X	L	L	H	H	↑	X	Input	← DOR →	b1 b2 b3 b4 b5 b6 b7 b8	b8	Reg. "A" will OR data from I/O and reg. "B"
7	H	H	H	L	X	↑	X	Hi-Z	a1 a2 a3 a4 a5 a6 a7 a8	a1 a2 a3 a4 a5 a6 a7 a8	a8	Transfer data down
8	L	H	H	L	X	↑	X	Output	a1 a2 a3 a4 a5 a6 a7 a8	a1 a2 a3 a4 a5 a6 a7 a8	a8	from reg. "A" to reg. "B"
9	X	L	H	L	X	↑	X	Input	I1 I2 I3 I4 I5 I6 I7 I8	a1 a2 a3 a4 a5 a6 a7 a8	a8	Entering data and transfer down
10	H	H	L	L	X	↑	X	Hi-Z	b1 b2 b3 b4 b5 b6 b7 b8	a1 a2 a3 a4 a5 a6 a7 a8	a8	(1) Exchange data between registers
11	L	H	L	L	X	↑	X	Output	b1 b2 b3 b4 b5 b6 b7 b8	a1 a2 a3 a4 a5 a6 a7 a8	a8	(2)
12	X	L	L	L	X	↑	X	Input	← DOR →	a1 a2 a3 a4 a5 a6 a7 a8	a8	(3) Beside data exchanging, reg. "A" will "OR" data from I/O and reg. "B"
13	H	H	H	H	L	↑	d	Hi-Z	a1 a2 a3 a4 a5 a6 a7 a8	d b1 b2 b3 b4 b5 b6 b7	b7	Serial shifting in the
14	L	H	H	H	L	↑	d	Output	a1 a2 a3 a4 a5 a6 a7 a8	d b1 b2 b3 b4 b5 b6 b7	b7	lower reg. "B"
15	X	L	H	H	L	↑	d	Input	I1 I2 I3 I4 I5 I6 I7 I8	d b1 b2 b3 b4 b5 b6 b7	b7	Entering data and serial shifting
16	H	H	L	H	L	↑	d	Hi-Z	b1 b2 b3 b4 b5 b6 b7 b8	d b1 b2 b3 b4 b5 b6 b7	b7	Transfer up and serial
17	L	H	L	H	L	↑	d	Output	b1 b2 b3 b4 b5 b6 b7 b8	d b1 b2 b3 b4 b5 b6 b7	b7	shifting
18	X	L	L	H	L	↑	d	Input	← DOR →	d b1 b2 b3 b4 b5 b6 b7	b7	DOR function and serial shifting

X = Don't care
Hi-Z/Output/Input = High impedance state/Output state/Input state
a1 ... a8/b1 ... b8 = The content of the upper register "A"/the lower shift register "B" before the most recent ↑ transition of the clock
I1 ... I8 = The level of steady state inputs of the I/O pins
DOR = "Data ORing function" ORing data from both I/O pins and register "B", i.e. I1+b1, I2+b2, I3+b3, ... I8+b8
d = Data of the serial input

timing diagram (example clock No. 1–7)



H/L = I/O Pins are outputs
1/O = I/O Pins are inputs

TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN74ALS962 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN74ALS962			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	all outputs			−2.6	mA
I_{OL}	Low-level output current	O_S			16	mA
		I/O1 thru I/O8			24	
f_{clock}	Clock frequency		0		25	MHz
Clock Pulse	High pulse width		25	17		ns
	Low pulse width		15	7		
t_{SET-UP}	Data set-up time	CLK↑ → I/O	10			ns
		CLK↑ → I_S	10			
t_{HOLD}	Data hold time		0			ns
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

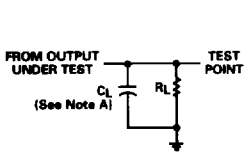
PARAMETER		TEST CONDITIONS		SN74ALS962 MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
V_{OH}	all outputs	V_{CC} = 4.5 V	I_{OH} = −2.6 mA	2.4	3.0		V
V_{OL}	OS	V_{CC} = 4.5 V	I_{OL} = 8 mA		0.25	0.4	V
			I_{OL} = 16 mA		0.35	0.5	
	I/O1 thru I/O8	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4	
			I_{OL} = 24 mA		0.35	0.5	
I_I	I/O1 thru I/O8	V_{CC} = 5.5 V	V_I = 5.5 V			0.1	mA
	Any other		V_I = 7 V			0.1	
I_{IH}*		V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}*		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
I_{IL} CLK		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2	mA
I_O§	all outputs	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		28	50	mA
			Outputs low		40	63	
			Outputs disabled		30	54	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
* For I/O ports (I/O1 through I/O8), the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}. Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

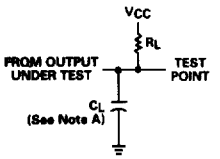
switching characteristics (V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX, C_L = 50 pF, R_L = 500 Ω)

PARAMETER			MIN	TYP	MAX	UNIT
f_{max}	Maximum Clock Frequency		25	30		MHz
t_{PLH}	Propagation Delay Time, Low-to-High-Level from Clock to Any Outputs		2	10	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level from Clock to Any Outputs		5	14	26	ns
t_{ENABLE}	Enable Time from Any Control Inputs		3	10	30	ns
$t_{DISABLE}$	Disable Time from Any Control Inputs		3	10	30	ns
t_{ZH}	Output Enable Time to High Level			12	30	ns
t_{ZL}	Output Enable to Low Level			12	30	ns
t_{HZ}	Output Disable Time from High Level			15	20	ns
t_{LZ}	Output Disable Time from Low Level			16	20	ns

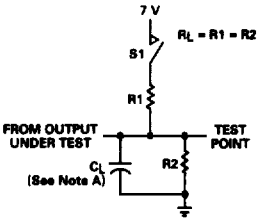
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR
STATE
TOTEM-POLE OUTPUTS

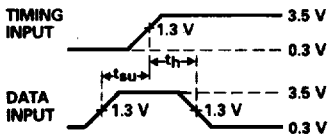


LOAD CIRCUIT FOR
OPEN-COLLECTOR OUTPUTS

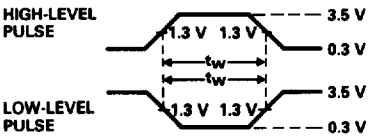


LOAD CIRCUIT FOR
THREE-STATE OUTPUTS

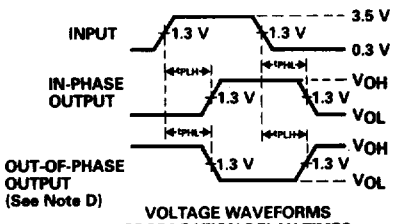
NOTE A: C_L includes probe and jig capacitance.



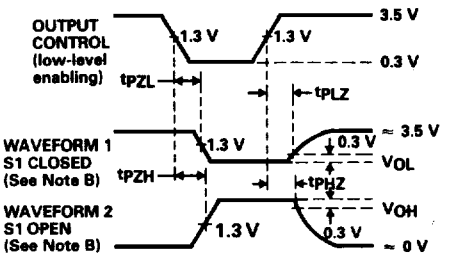
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. When measuring propagation delay items of 3-state outputs, switch S1 is open.
E. The outputs are measured one at a time with one input transition per measurement.