MN4520B/MN4520BS

Dual 4-Bit Binary Counter

■ Outline

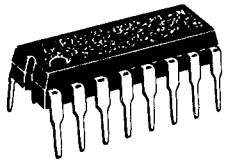
The MN4520B/S consists of two independent 4-bit binary UP counters.

When the level of the $\overline{CP}_1$ clock is "H", the counter advances at the rise of the CP_0 clock, and when the level of the CP_0 clock is "L", the counter advances at the fall of the $\overline{CP}_1$ clock.

When the level of the reset input is set to "H", the respective counter is reset ($O_0 \sim O_3 = L$) irrespectively of the other inputs.

This dual 4-bit binary counter is equivalent to Motorola's MC14520B and RCA's CD4520B.

P-3



16-pin plastic DIL package

P-4

16-pin PANAFLAT package (SO-16D)

■ Truth Table

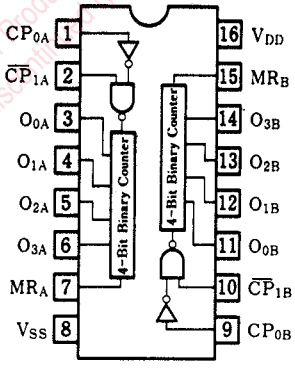
CP_0	$\overline{CP}_1$	MR	Operation Mode
↓	H	L	Countable
L	↓	L	
↓	×	L	No Change
×	↓	L	
↓	L	L	
H	↓	L	
×	×	H	$O_0 \sim O_3 = L$

Note) ×: don't care

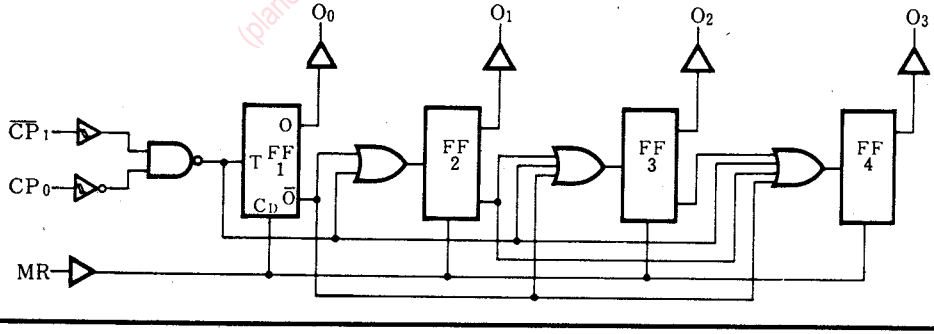
Pin description

$CP_{0A} \sim CP_{0B}$: Positive clock input (↓)
$\overline{CP}_{1A} \sim \overline{CP}_{1B}$: Negative clock input (↓)
MR_A, MR_B : Reset input
$O_{0A} \sim O_{3A}$: BCD output (4 bits)
$O_{0B} \sim O_{3B}$: BCD output (4 bits)

Pin Configuration



■ Logic Diagram



■ Absolute Maximum Ratings (Ta=25°C)

Item		Symbol	Rating	Unit
Supply voltage		V_{DD}	−0.5~+18	V
Input voltage		V_I	−0.5~V_{DD}+0.5*	V
Output pin voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak input · output pin current		$\pm I_I$	max. 10	mA
Power dissipation (per package)	Ta=−40~+60°C	P_D	max. 400	mW
	Ta=+60~+80°C		Decrease to 200mW at the rate of 8mW/°C	
Power dissipation (per output pin)		P_D	max. 100	mW
Operating ambient temperature		T_{opr}	−40~+85	°C
Storage temperature		T_{stg}	−65~+150	°C

* V_{DD}+0.5V should be lower than 18V.

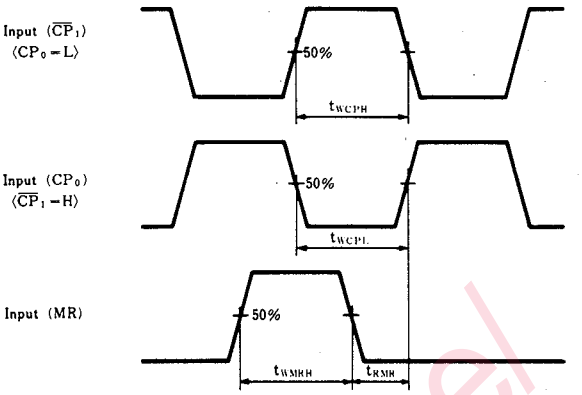
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Condition		Ta=−40°C min.	Ta=−40°C max.	Ta=25°C min.	Ta=25°C max.	Ta=85°C min.	Ta=85°C max.	Unit
Static supply current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output voltage low level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		$\|I_O\|$<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output voltage high level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		$\|I_O\|$<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input voltage low level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input voltage high level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output current low level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output current high level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output current high level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input leakage current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

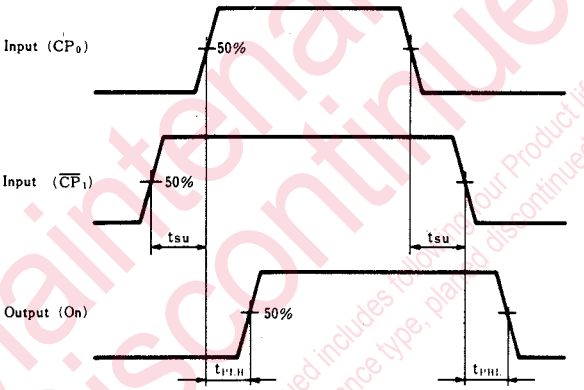
■ Switching Characteristics (Ta=25°C, V_{SS}=0V, C_L=50pF)

Item	V_{DD}(V)	Symbol	min.	typ.	max.	Unit
Output rise time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output fall time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation time CP_0, $\overline{CP}_1$→On (L→H)	5	t_{PLH}	—	145	435	ns
	10		—	65	195	
	15		—	50	150	
Propagation time CP_0, $\overline{CP}_1$→On (H→L)	5	t_{PHL}	—	170	510	ns
	10		—	75	225	
	15		—	50	150	
Propagation time MR→On (H→L)	5	t_{PHL}	—	145	435	ns
	10		—	60	180	
	15		—	45	135	
Low level minimum CP_0 clock pulse width	5	t_{WCPL}	—	85	255	ns
	10		—	30	90	
	15		—	25	75	
High level minimum $\overline{CP}_1$ clock pulse width	5	t_{WCPH}	—	85	255	ns
	10		—	30	90	
	15		—	25	75	
High level minimum reset pulse width	5	t_{WMRH}	—	45	135	ns
	10		—	20	60	
	15		—	15	45	
Reset recovery time	5	t_{RMR}	—	25	75	ns
	10		—	15	45	
	15		—	10	30	
Set-up time CP_0→$\overline{CP}_1$	5	t_{su}	—	90	270	ns
	10		—	35	105	
	15		—	25	75	
Set-up time $\overline{CP}_1$→CP_0	5	t_{su}	—	75	225	ns
	10		—	30	90	
	15		—	20	60	
Maximum clock frequency	5	f_{max}	3	6	—	MHz
	10		7	15	—	
	15		10	21	—	
Input capacitance		C_I	—	—	7.5	pF

• Switching waveforms

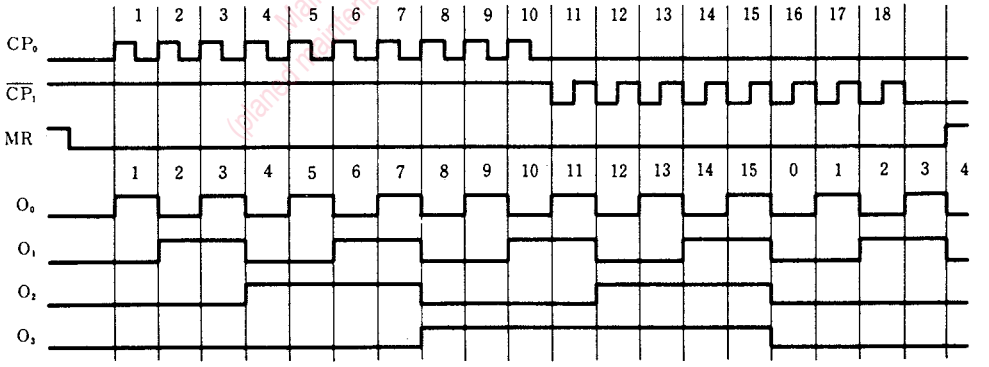


Waveforms showing recovery time for MR; minimum CP_0, $\overline{CP}_1$ and MR pulse widths.



Waveforms showing set-up times for CP_0 to $\overline{CP}_1$ and $\overline{CP}_1$ to CP_0, and propagation delays.

■ Timing Diagram



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