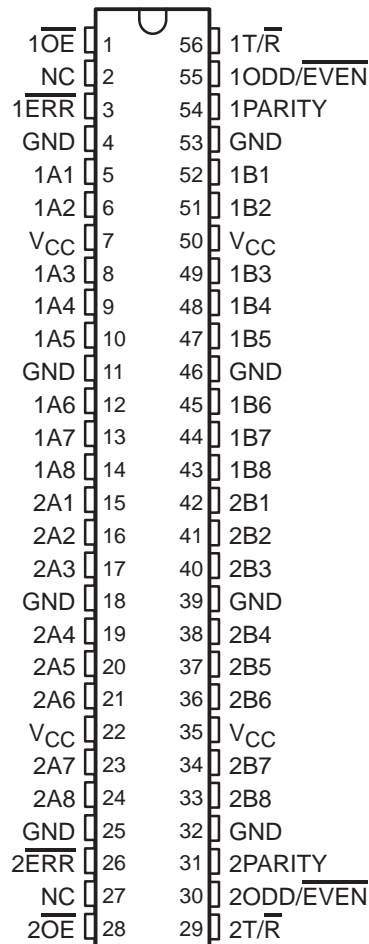


SN54ABT16657, SN74ABT16657 16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

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- **Members of the Texas Instruments Widebus™ Family**
- **State-of-the-Art EPIC-II B™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5 V, T_A = 25^\circ C$**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs ($-32\text{-mA } I_{OH}, 64\text{-mA } I_{OL}$)**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABT16657 . . . WD PACKAGE
SN74ABT16657 . . . DGG OR DL PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'ABT16657 contain two noninverting octal transceiver sections with separate parity generator/checker circuits and control signals. For either section, the transmit/receive ($1T/\bar{R}$ or $2T/\bar{R}$) input determines the direction of data flow. When $1T/\bar{R}$ (or $2T/\bar{R}$) is high, data flows from the 1A (or 2A) port to the 1B (or 2B) port (transmit mode); when $1T/\bar{R}$ (or $2T/\bar{R}$) is low, data flows from the 1B (or 2B) port to the 1A (or 2A) port (receive mode). When the output-enable ($1OE$ or $2OE$) input is high, both the 1A (or 2A) and 1B (or 2B) ports are in the high-impedance state.

Odd or even parity is selected by a logic high or low level, respectively, on the $1ODD/\overline{EVEN}$ (or $2ODD/\overline{EVEN}$) input. $1PARITY$ (or $2PARITY$) carries the parity bit value; it is an output from the parity generator/checker in the transmit mode and an input to the parity generator/checker in the receive mode.

In the transmit mode, after the 1A (or 2A) bus is polled to determine the number of high bits, $1PARITY$ (or $2PARITY$) is set to the logic level that maintains the parity sense selected by the level at the $1ODD/\overline{EVEN}$ (or $2ODD/\overline{EVEN}$) input. For example, if $1ODD/\overline{EVEN}$ is low (even parity selected) and there are five high bits on the 1A bus, then $1PARITY$ is set to the logic high level so that an even number of the nine total bits (eight 1A-bus bits plus parity bit) are high.



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description (continued)

In the receive mode, after the 1B (or 2B) bus is polled to determine the number of high bits, the $1\overline{ERR}$ (or $2\overline{ERR}$) output logic level indicates whether or not the data to be received exhibits the correct parity sense. For example, if $1\text{ODD}/\overline{\text{EVEN}}$ is high (odd parity selected), 1PARITY is high, and there are three high bits on the 1B bus, then $1\overline{ERR}$ is low, indicating a parity error.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16657 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT16657 is characterized for operation from -40°C to 85°C .

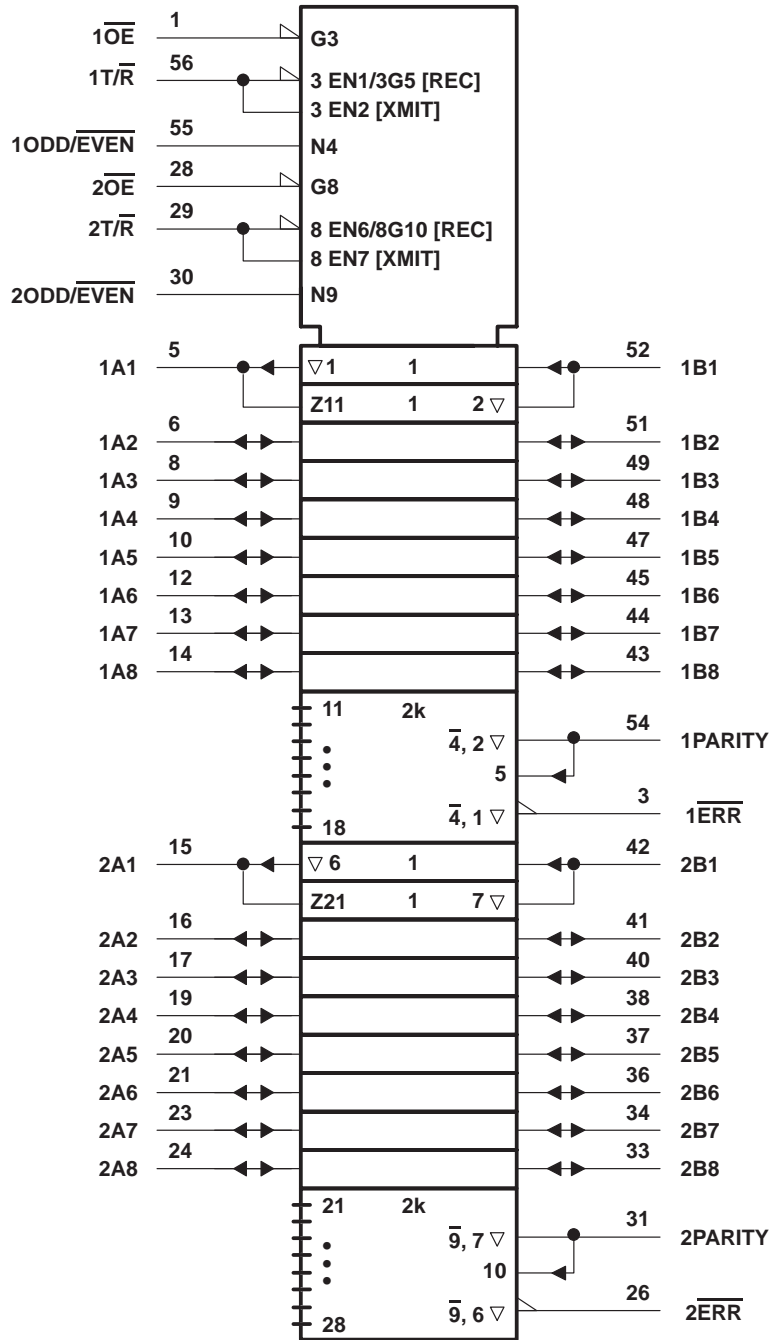
FUNCTION TABLE
(each 8-bit section)

NUMBER OF A OR B INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT PARITY	OUTPUTS	
	\overline{OE}	$\text{T}/\overline{\text{R}}$	$\text{ODD}/\overline{\text{EVEN}}$		$\overline{\text{ERR}}$	OUTPUT MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	L	H
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	L
Don't care	H	X	X	Z	Z	Z

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logic symbol†

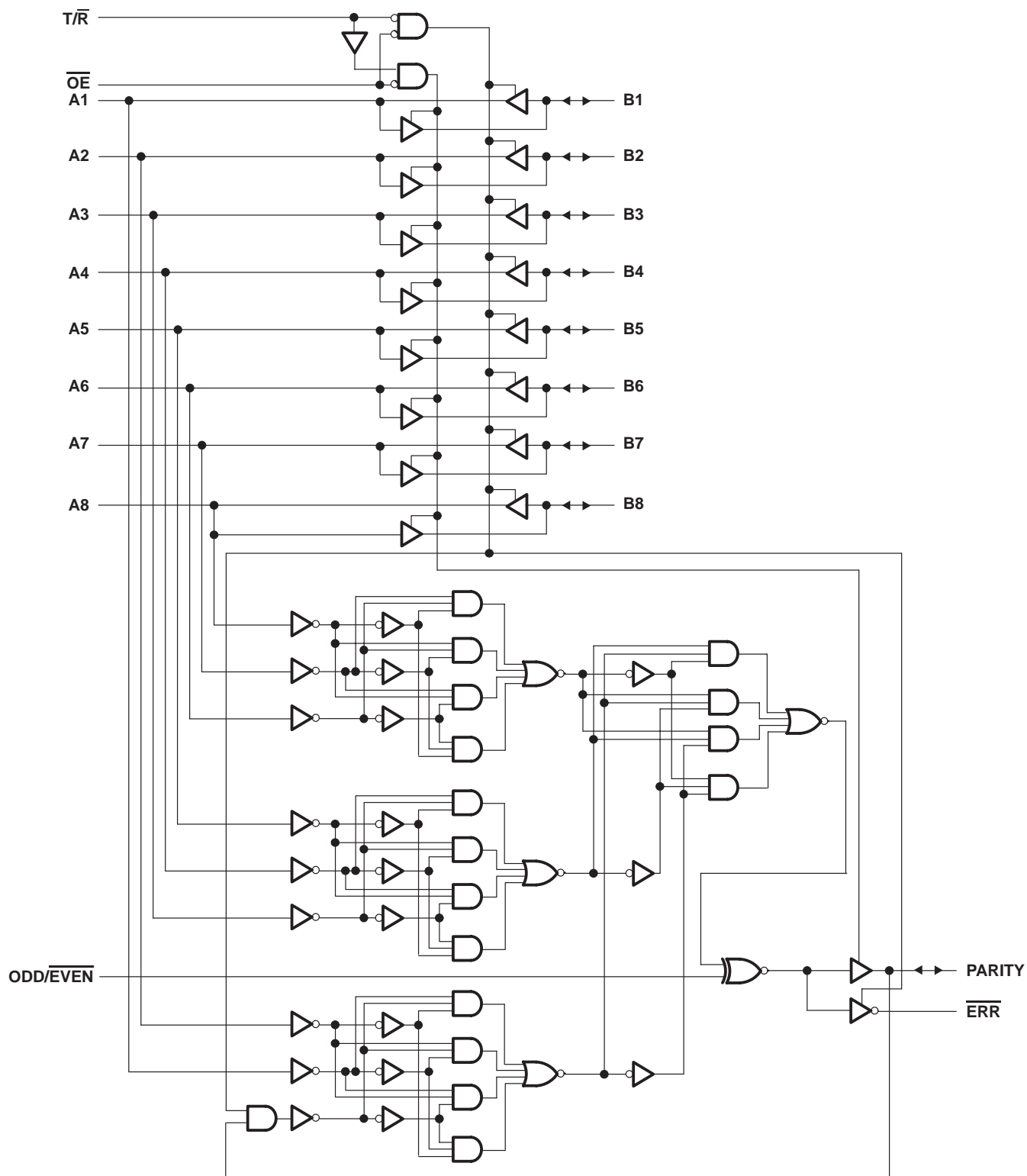


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54ABT16657, SN74ABT16657
16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS
AND 3-STATE OUTPUTS

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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT16657	96 mA
SN74ABT16657	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	81°C/W
DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

		SN54ABT16657		SN74ABT16657		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

SN54ABT16657, SN74ABT16657 16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT16657		SN74ABT16657		UNIT	
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V	
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA			2.5		2.5		2.5	V	
	V _{CC} = 5 V, I _{OH} = -3 mA			3		3		3		
	V _{CC} = 4.5 V	I _{OH} = -24 mA			2		2			
I _{OH} = -32 mA				2*				2		
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 24 mA				0.55		0.55	V	
		I _{OL} = 64 mA				0.55*		0.55		
V _{hys}				100					mV	
I _I	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA
	A or B ports				±100		±100		±100	
I _{OZH} ‡	V _{CC} = 5.5 V, V _O = 2.7 V			50		50		50	μA	
I _{OZL} ‡	V _{CC} = 5.5 V, V _O = 0.5 V			-50		-50		-50	μA	
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100		±450		±100	μA	
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high				50		50	μA	
I _O §	V _{CC} = 5.5 V, V _O = 2.5 V			-50	-100	-180		-50	-180	mA
I _{CC}	A or B ports	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high			2		2	2	mA
			Outputs low			36		36	36	
			Outputs disabled			2		2	2	
ΔI _{CC} ¶		V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND				50		50	μA	
C _i	Control inputs	V _I = 2.5 V or 0.5 V				3			pF	
C _{iO}	A or B ports	V _O = 2.5 V or 0.5 V				9			pF	

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54ABT16657		SN74ABT16657		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	2.5	3.3	1.5	4.2	1.5	4.1	ns
t_{PHL}			2	3.1	3.9	2	4.5	2	4.3	
t_{PLH}	A	PARITY	2	4.6	5.4	2	7	2	6.7	ns
t_{PHL}			2	4.3	5.1	2	6.5	2	6.1	
t_{PLH}	ODD/EVEN	PARITY, \overline{ERR}	2	4.6	5.4	2	7	2	6.7	ns
t_{PHL}			2	4.3	5.1	2	6.5	2	6.1	
t_{PLH}	B	\overline{ERR}	2	4.6	5.4	2	7	2	6.7	ns
t_{PHL}			2	4.3	5.1	2	6.5	2	6.1	
t_{PLH}	PARITY	\overline{ERR}	2	4.6	5.4	2	7	2	6.7	ns
t_{PHL}			2	4.3	5.1	2	6.5	2	6.1	
t_{PZH}	\overline{OE}	A or B	2	3.9	4.9	2	5.8	2	5.6	ns
t_{PZL}			2.5	4.3	5.1	2.5	6.2	2.5	6	
t_{PHZ}	\overline{OE}	A or B	2	3.6	4.5	2	5.5	2	5.4	ns
t_{PLZ}			1.5	3	3.8	1.5	4.7	1.5	4.3	
t_{PZH}	\overline{OE}	PARITY, \overline{ERR}	2	4	4.9	2	5.8	2	5.6	ns
t_{PZL}			2.5	4.1	5.1	2.5	6.2	2.5	6	
t_{PHZ}	\overline{OE}	PARITY, \overline{ERR}	1	3.5	4.5	1	5.5	1	5.4	ns
t_{PLZ}			1.5	3	3.8	1.5	4.7	1.5	4.3	

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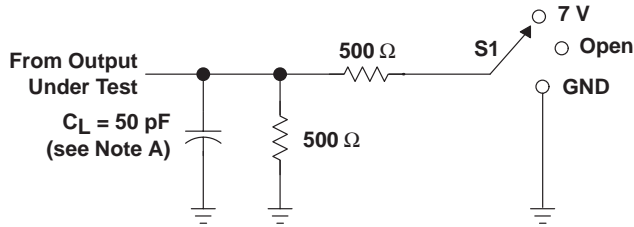


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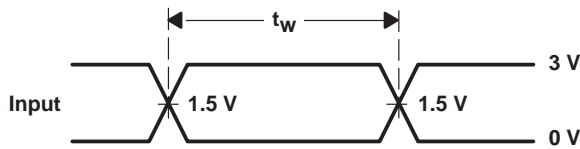
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PARAMETER MEASUREMENT INFORMATION

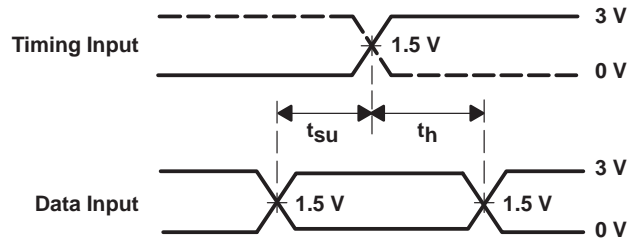


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

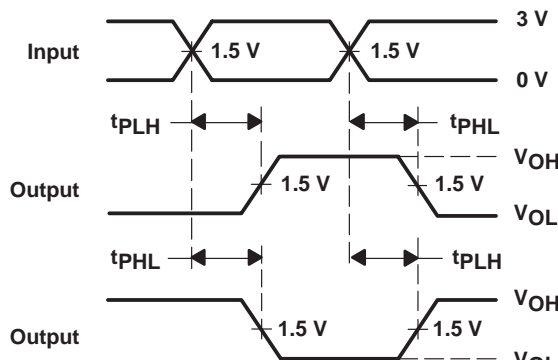
LOAD CIRCUIT



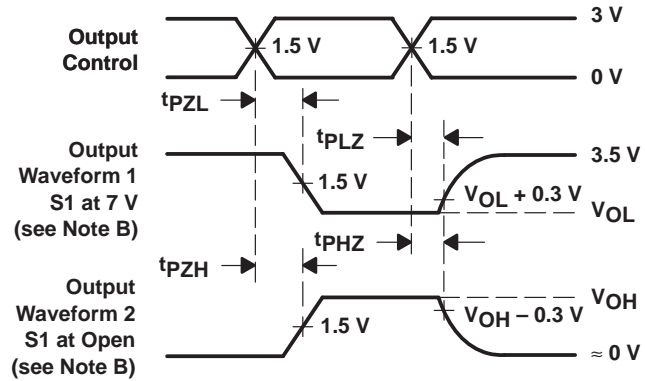
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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