

# MM54C165/MM74C165 Parallel-Load 8-Bit Shift Register

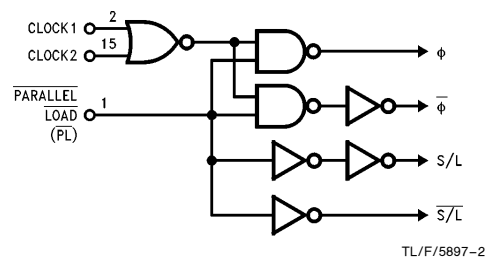
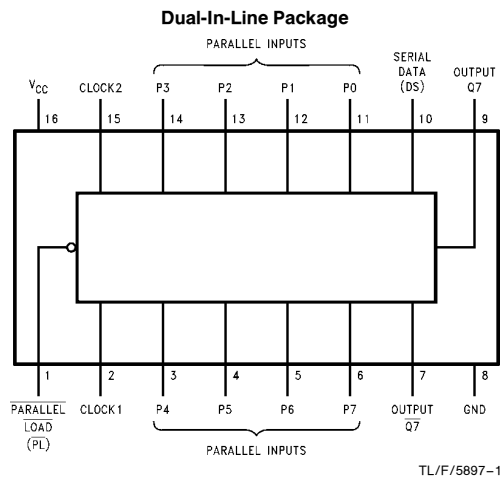
## General Description

The MM54C165/MM74C165 functions as an 8-bit parallel-load, serial shift register. Data is loaded into the register independent of the state of the clock(s) when PARALLEL LOAD (PL) is low. Shifting is inhibited as long as PL is low. Data is sequentially shifted from complementary outputs, Q<sub>7</sub> and Q<sub>7</sub>, highest-order bit (P7) first. New serial data may be entered via the SERIAL DATA (Ds) input. Serial shifting occurs on the rising edge of CLOCK1 or CLOCK2. Clock inputs may be used separately or together for combined clocking from independent sources. Either clock input may be used also as an active-low clock enable. To prevent double-clocking when a clock input is used as an enable, the enable must be changed to a high level (disabled) only while the clock is high.

## Features

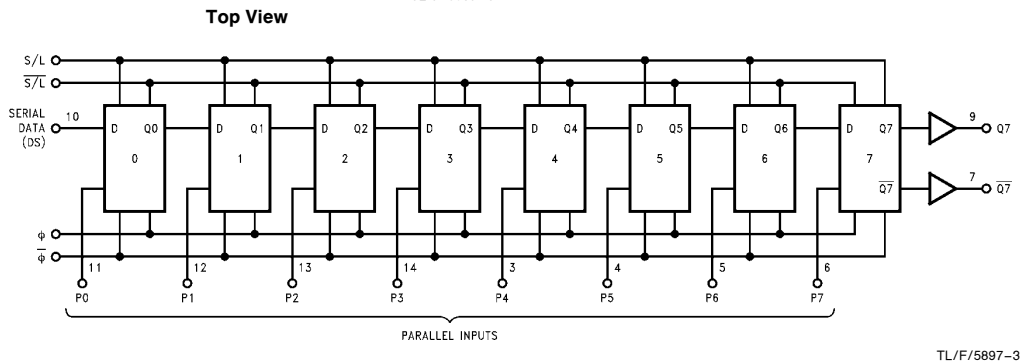
- Wide supply voltage range 3V to 15V
- Guaranteed noise margin 1V
- High noise immunity 0.45 V<sub>CC</sub> (typ.)
- Low power TTL compatibility fan out of 2  
driving 74L
- Parallel loading independent of clock
- Dual clock inputs
- Fully static operation

## Connection and Block Diagrams



Order Number MM54C165\* or MM74C165\*

\*Please look into Section 8, Appendix D for availability of various package types.



MM54C165/MM74C165 Parallel-Load 8-Bit Shift Register

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	-0.3V to $V_{CC} + 0.3V$
Operating Temperature Range	-55°C to +125°C
MM54C165	-40°C to +85°C
MM74C165	

Storage Temperature Range	-65°C to +150°C
Absolute Maximum $V_{CC}$	18V
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating $V_{CC}$ Range	3V to 15V
Lead Temperature (Soldering, 10 sec.)	260°C

## DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>CMOS TO CMOS</b>						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V, I_O = -10 \mu A$ $V_{CC} = 10V, I_O = -10 \mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V, I_O = +10 \mu A$ $V_{CC} = 10V, I_O = +10 \mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	$\mu A$
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		$\mu A$
$I_{CC}$	Supply Current	$V_{CC} = 15V$		0.05	300	$\mu A$
<b>CMOS TO LPTTL INTERFACE</b>						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5V, I_O = -360 \mu A$ 74C $V_{CC} = 4.75V, I_O = -360 \mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC} = 4.5V, I_O = 360 \mu A$ 74C $V_{CC} = 4.75V, I_O = 360 \mu A$			0.4 0.4	V V
<b>OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (short circuit current)</b>						
$I_{SOURCE}$	Output Source Current (P-Channel)	$V_{CC} = 5V$ $T_A = 25^\circ C, V_{OUT} = 0V$	-1.75	-3.3		mA
$I_{SOURCE}$	Output Source Current (P-Channel)	$V_{CC} = 10V$ $T_A = 25^\circ C, V_{OUT} = 0V$	-8.0	-15		mA
$I_{SINK}$	Output Sink Current (N-Channel)	$V_{CC} = 5V$ $T_A = 25^\circ C, V_{OUT} = V_{CC}$	1.75	3.6		mA
$I_{SINK}$	Output Sink Current (N-Channel)	$V_{CC} = 10V$ $T_A = 25^\circ C, V_{OUT} = V_{CC}$	8.0	16		mA

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

## AC Electrical Characteristics\* $T_A = 25^\circ\text{C}$ , $C_L = 50\text{ pF}$ , unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{pd0}$ , $t_{pd1}$	Propagation Delay Time to a Logical "0" or Logical "1" from Clock or Load to Q or $\bar{Q}$	$V_{CC} = 5\text{V}$		200	400	ns
		$V_{CC} = 10\text{V}$		80	200	ns
$t_{pd0}$ , $t_{pd1}$	Propagation Delay Time to a Logical "0" or Logical "1" from H to Q or $\bar{Q}$	$V_{CC} = 5\text{V}$		200	400	ns
		$V_{CC} = 10\text{V}$		80	200	ns
$t_S$	Clock Inhibit Set-up Time	$V_{CC} = 5\text{V}$	150	75		ns
		$V_{CC} = 10\text{V}$	60	30		ns
$t_S$	Serial Input Set-up Time	$V_{CC} = 5\text{V}$	50	25		ns
		$V_{CC} = 10\text{V}$	30	15		ns
$t_H$	Serial Input Hold Time	$V_{CC} = 5\text{V}$	50	0		ns
		$V_{CC} = 10\text{V}$	30	0		ns
$t_S$	Parallel Input Set-Up Time	$V_{CC} = 5\text{V}$	150	75		ns
		$V_{CC} = 10\text{V}$	60	30		ns
$t_H$	Parallel Input Hold Time	$V_{CC} = 5\text{V}$	50	0		ns
		$V_{CC} = 10\text{V}$	30	0		ns
$t_W$	Minimum Clock Pulse Width	$V_{CC} = 5\text{V}$		70	200	ns
		$V_{CC} = 10\text{V}$		30	100	ns
$t_W$	Minimum Load Pulse Width	$V_{CC} = 5\text{V}$		85	180	ns
		$V_{CC} = 10\text{V}$		30	90	ns
$f_{MAX}$	Maximum Clock Frequency	$V_{CC} = 5\text{V}$	2.5	6		MHz
		$V_{CC} = 10\text{V}$	5	12		MHz
$t_r$ , $t_f$	Maximum Clock Rise and Fall Time	$V_{CC} = 5\text{V}$	10			$\mu\text{s}$
		$V_{CC} = 10\text{V}$	5			$\mu\text{s}$
$C_{IN}$	Input Capacitance	(Note 2)		5		pF
$C_{PD}$	Power Dissipation Capacitance	(Note 3)		65		pF

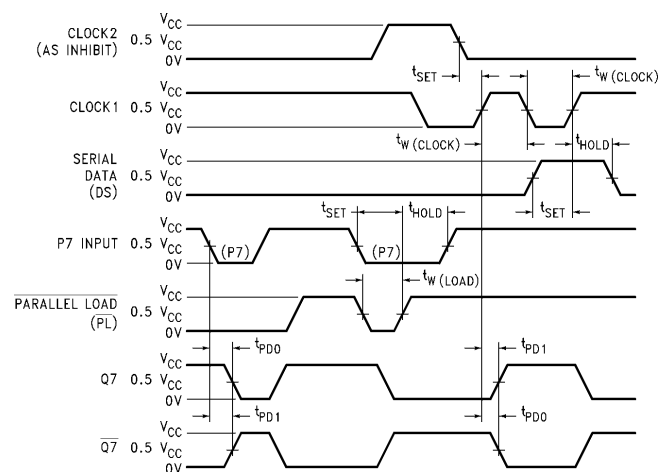
\*AC Parameters are guaranteed by DC correlated testing.

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** Capacitance is guaranteed by periodic testing.

**Note 3:**  $C_{PD}$  determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

## Switching Time Waveform



**Note A:** The remaining six data and the serial input are low.

**Note B:** Prior to test, high level data is loaded into the P7 input.

TL/F/5897-4

## Truth Table

State	Inputs					Internal		Outputs	
	$\overline{PL}$	Clock1	Clock2 (as enable)	Ds	P0 thru P7	Q0	Q1	Q7	$\overline{Q7}$
Parallel Load	L	X	X	X	P0...P7	P0	P1	P7	$\overline{P7}$
Enable	H	L	L	X	X	P0	P1	P7	$\overline{P7}$
Shift (with Ds)	H	↑	L	H	X	H	P0	P6	$\overline{P6}$
Shift (with Ds)	H	↑	L	L	X	L	H	P5	$\overline{P5}$
Hold (Disable)	H	↑	H	X	X	L	H	P5	$\overline{P5}$

X = don't care

H =  $V_{IN(1)}$

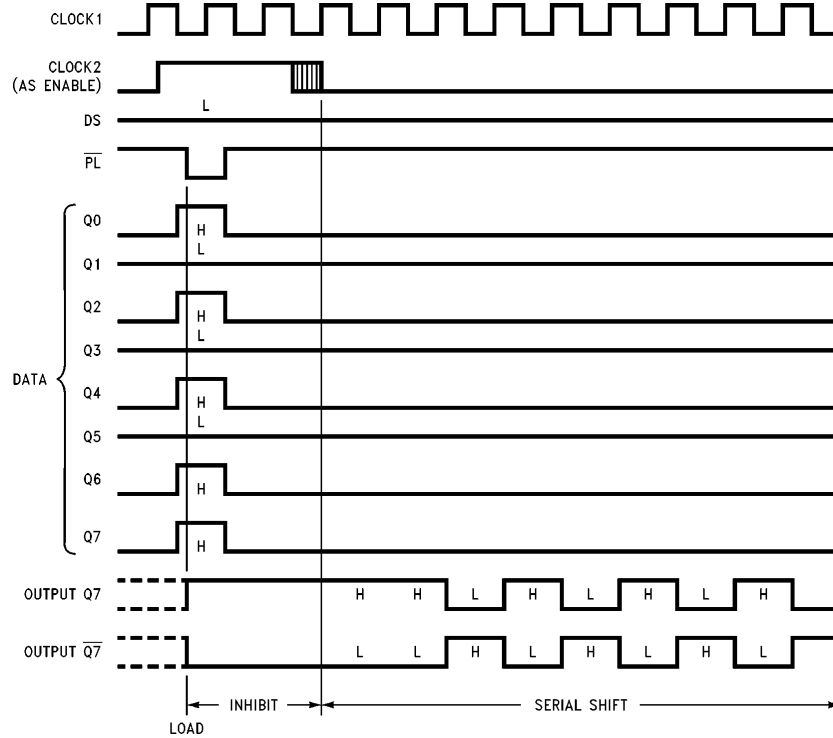
L =  $V_{IN(0)}$

↑ = clock transition from  $V_{IN(0)}$  to  $V_{IN(1)}$

P0 thru P7 = data present (and loaded into) parallel inputs

Q0 thru Q6 = Internal flip-flop outputs

## Logic Waveform



TL/F/5897-5

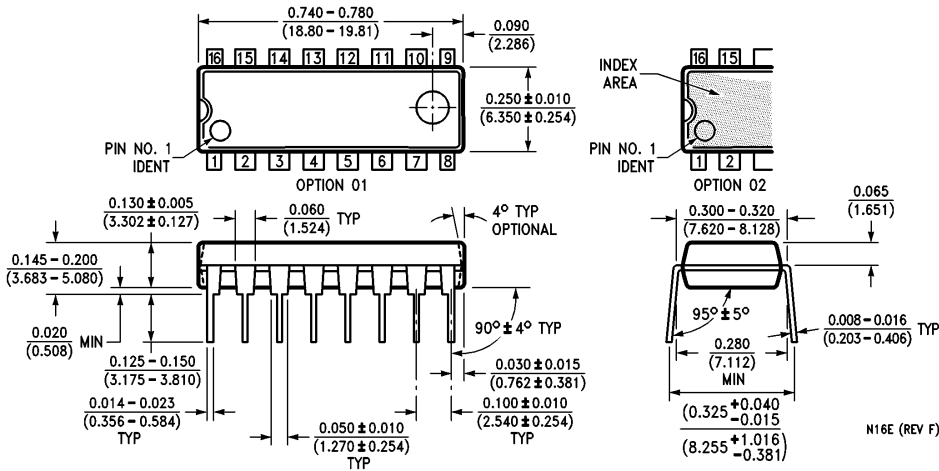
**Physical Dimensions** inches (millimeters)



**Ceramic Dual-In-Line Package (J)**  
**Order Number MM54C165J or MM74C165J**  
**NS Package Number J16A**

J16A (REV L)

**Physical Dimensions** inches (millimeters) (Continued)



**Molded Dual-In-Line Package (N)**  
**Order Number MM54C165N or MM74C165N**  
**NS Package Number N16E**

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