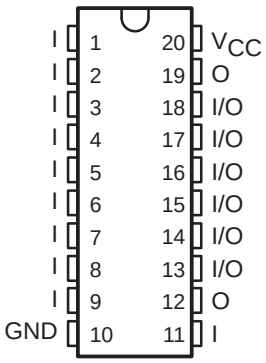
- **Choice of Operating Speeds**
  - **High-Speed, A Devices . . . 25 MHz Min**
  - **Half-Power, A-2 Devices . . . 16 MHz Min**
- **Choice of Input/Output Configuration**
- **Package Options Include Both Ceramic DIP and Chip Carrier in Addition to Ceramic Flat Package**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state buffers)	4
PAL16R6	8	0	6 (3-state buffers)	2
PAL16R8	8	0	8 (3-state buffers)	0

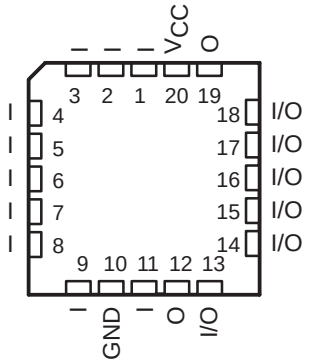
PAL16L8'
J OR W PACKAGE

(TOP VIEW)



PAL16L8'
FK PACKAGE

(TOP VIEW)



description

These programmable array logic devices feature high speed and a choice of either standard or half-power devices. They combine Advanced Low-Power Schottky technology with proven titanium-tungsten fuses. These devices will provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allow for quick design of "custom" functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

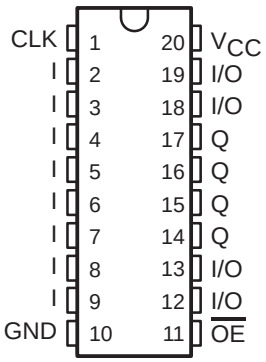
The Half-Power versions offer a choice of operating frequency, switching speeds, and power dissipation. In many cases, these Half-Power devices can result in significant power reduction from an overall system level.

The PAL16' M series is characterized for operation over the full military temperature range of –55°C to 125°C.

PAL is a registered trademark of Advanced Micro Devices Inc.

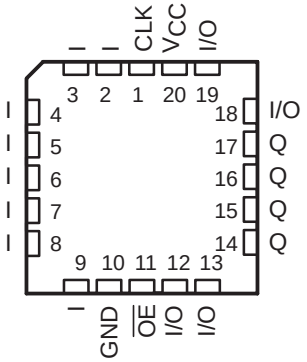
PAL16R4'
J OR W PACKAGE

(TOP VIEW)



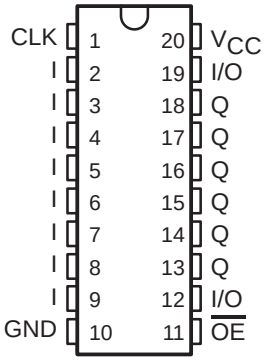
PAL16R4'
FK PACKAGE

(TOP VIEW)



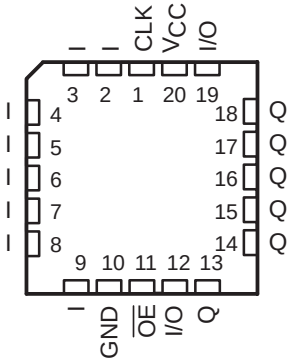
PAL16R6'
J OR W PACKAGE

(TOP VIEW)



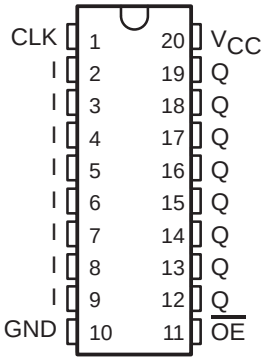
PAL16R6'
FK PACKAGE

(TOP VIEW)



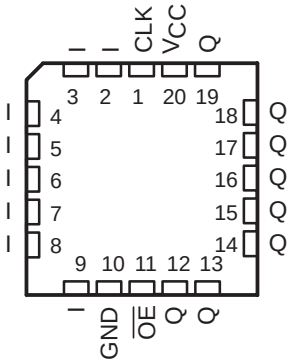
PAL16R8'
J OR W PACKAGE

(TOP VIEW)



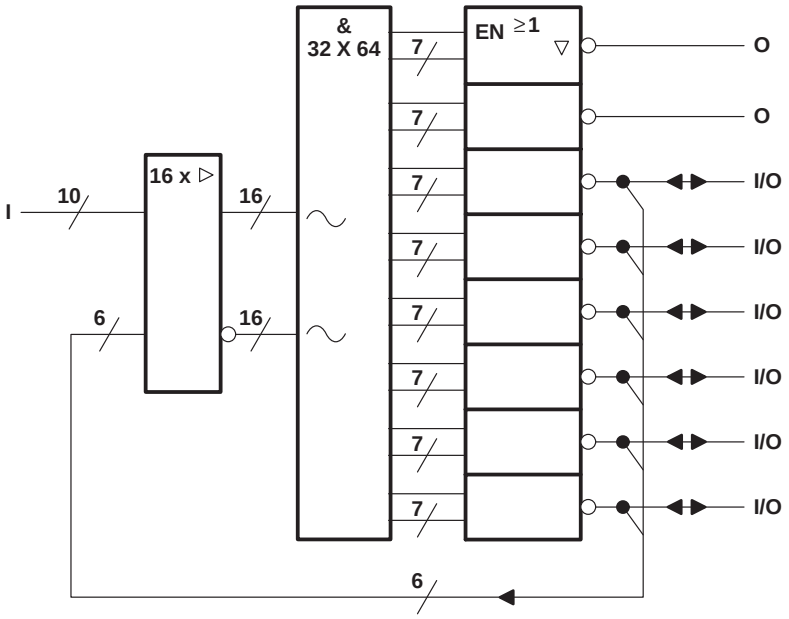
PAL16R8'
FK PACKAGE

(TOP VIEW)

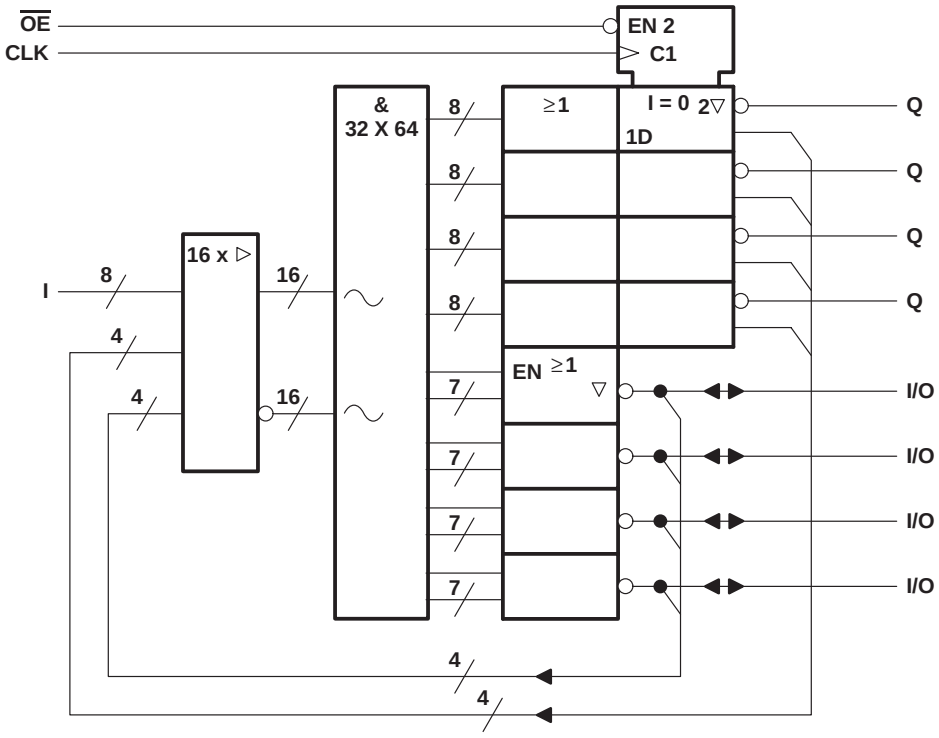


functional block diagrams (positive logic)

PAL16L8AM
PAL16L8A-2M



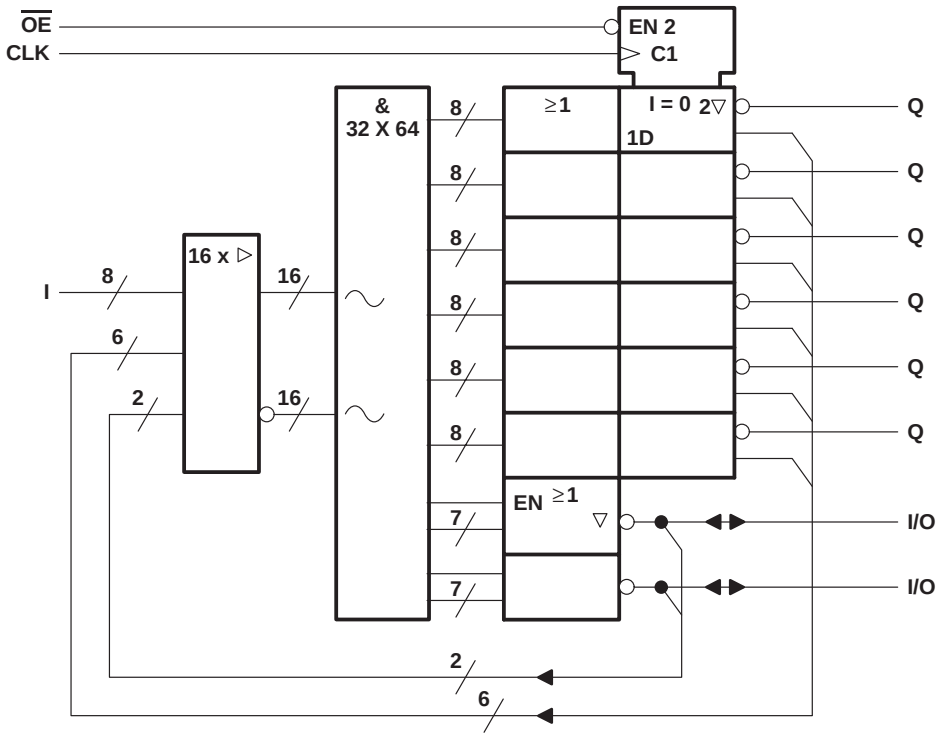
PAL16R4AM
PAL16R4A-2M



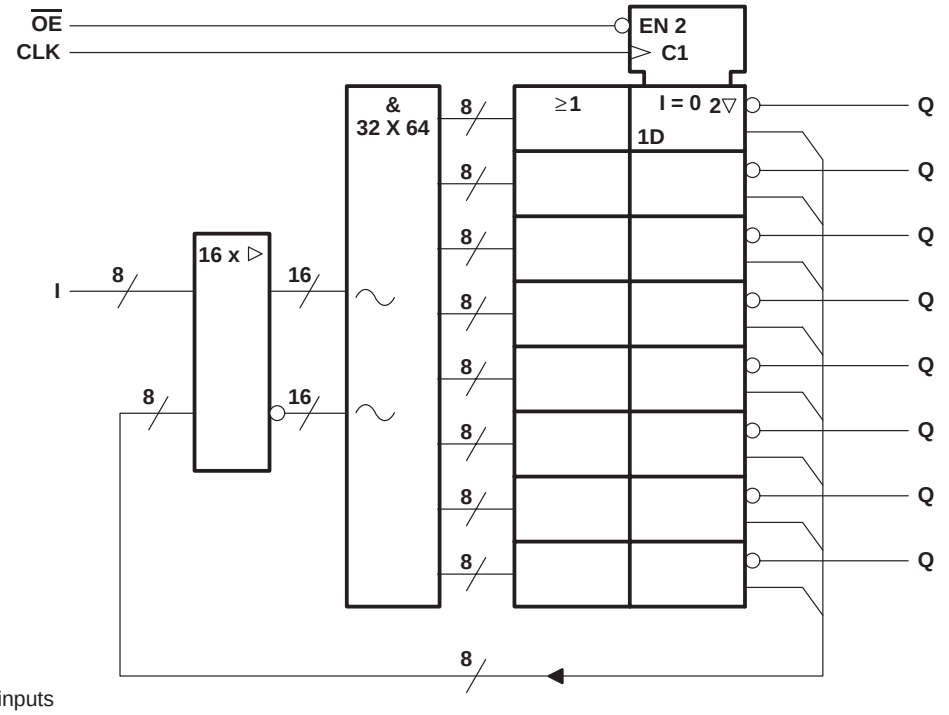
denotes fused inputs

functional block diagrams (positive logic)

PAL16R6AM
PAL16R6A-2M

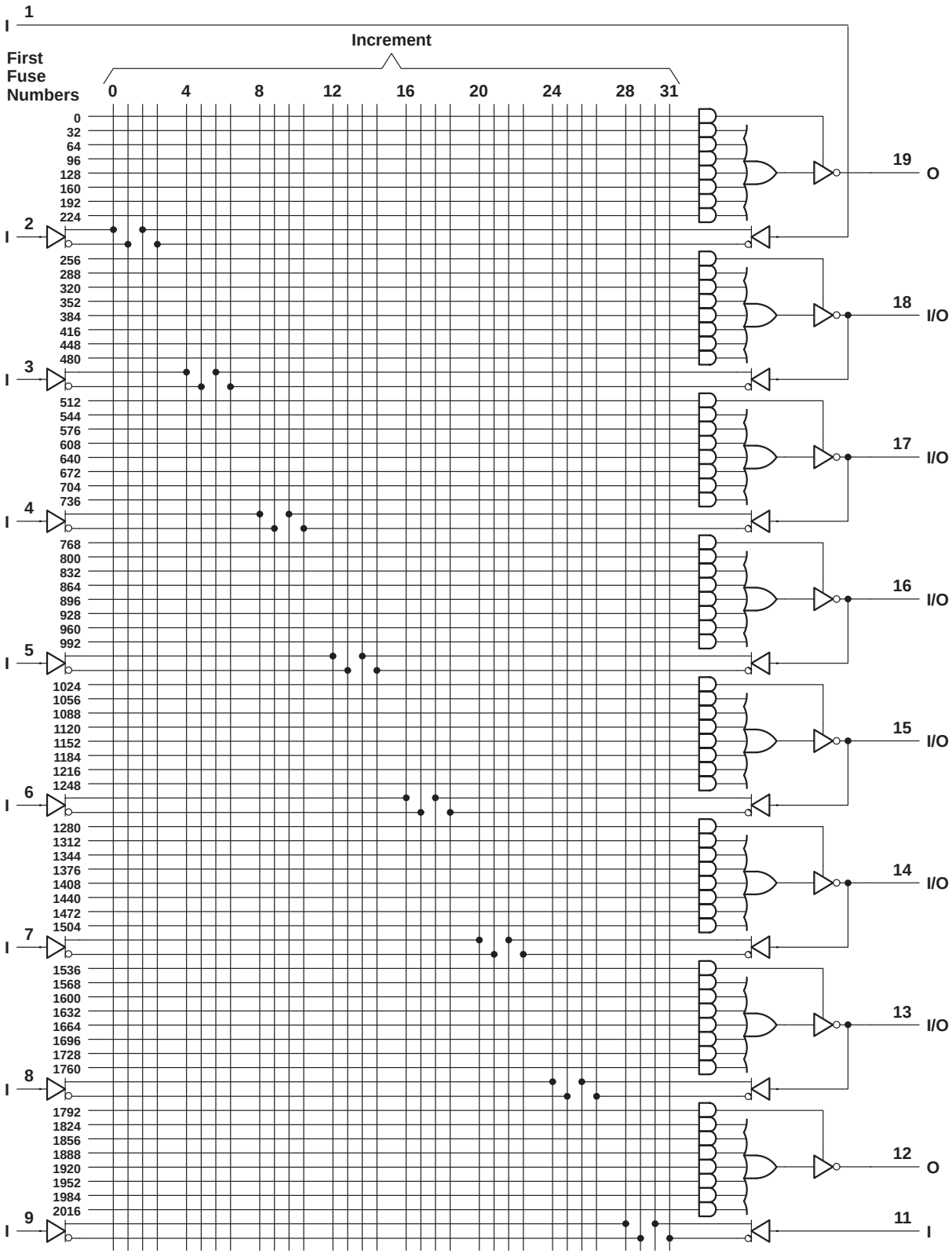


PAL16R8AM
PAL16R8A-2M



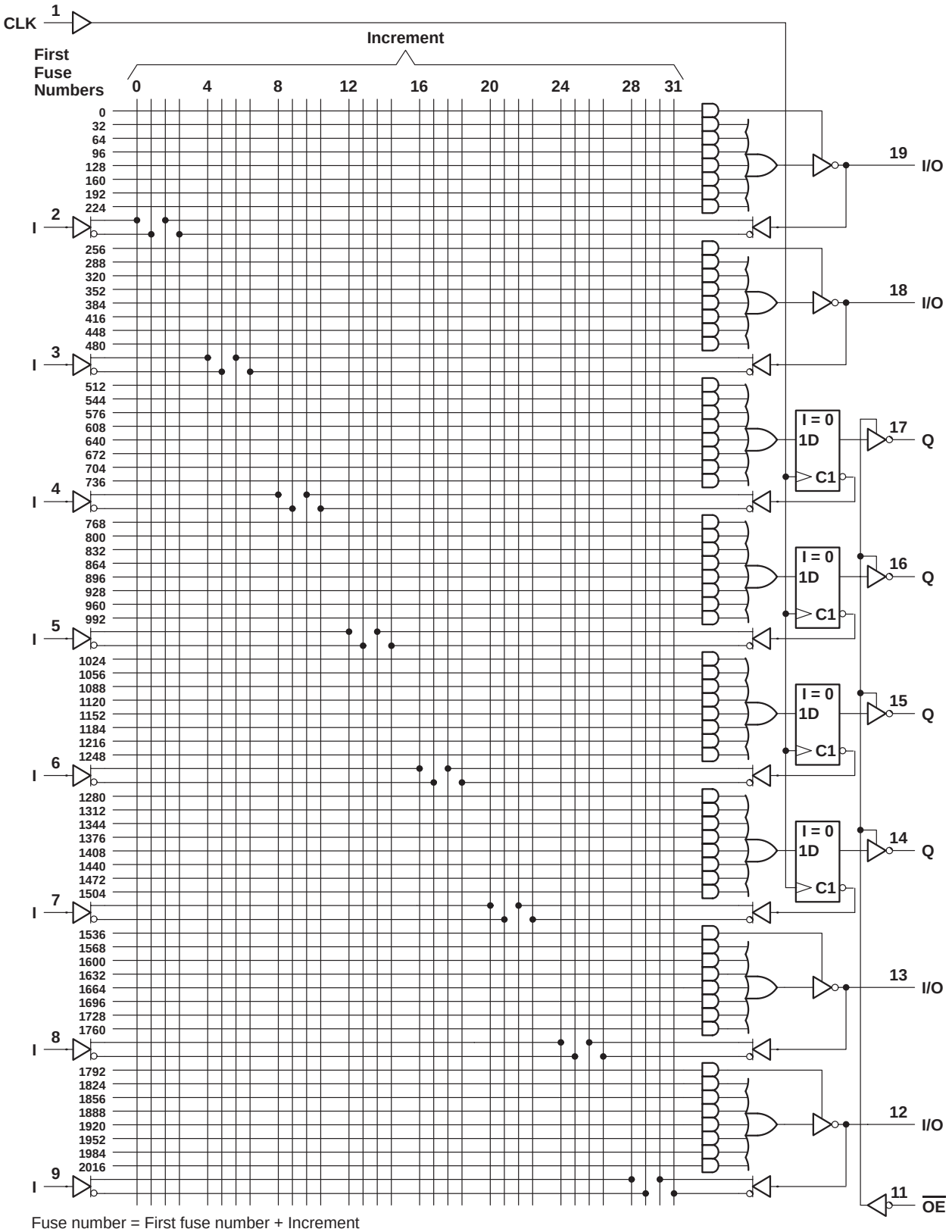
denotes fused inputs

logic diagram (positive logic)



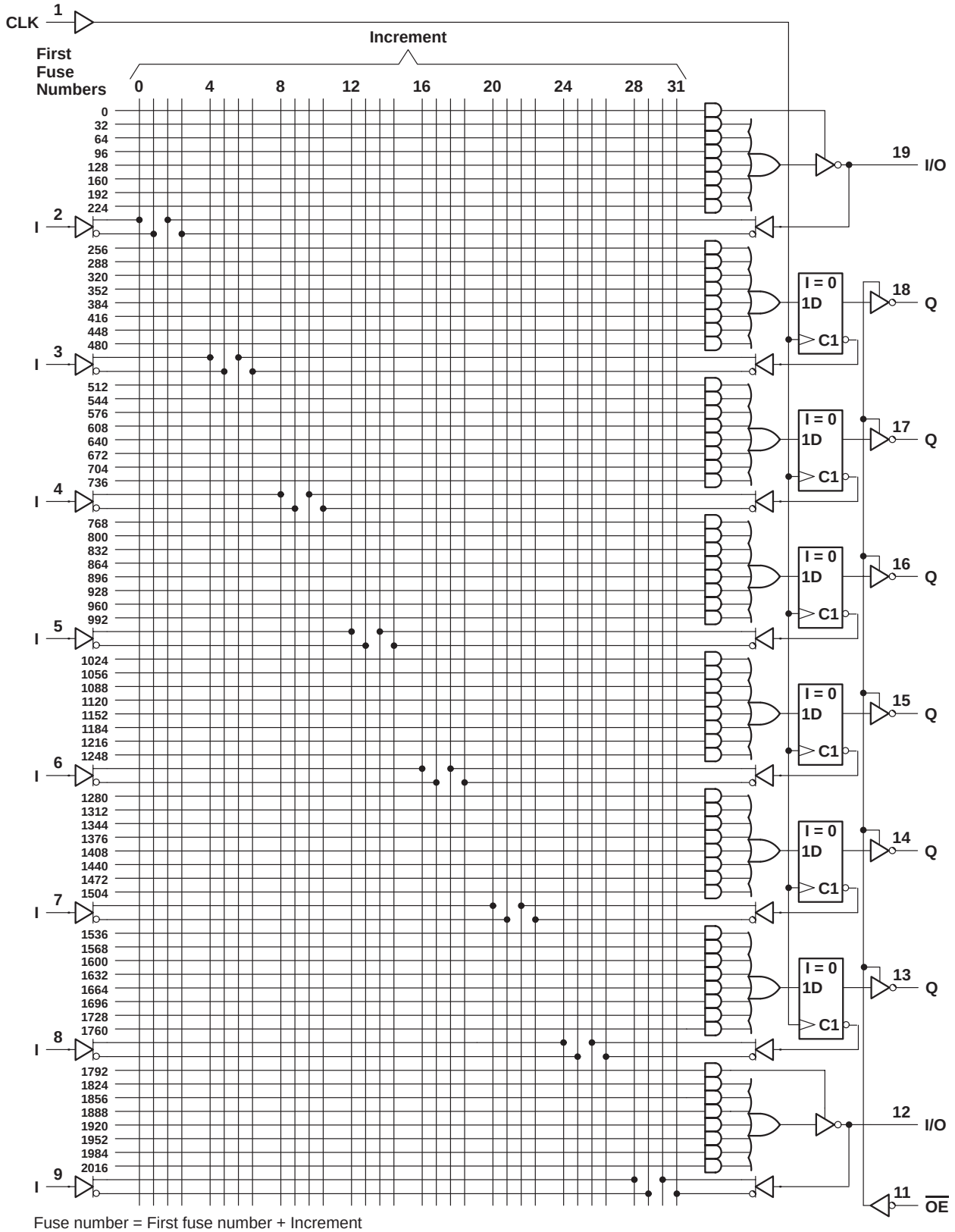
Fuse number = First fuse number + Increment

logic diagram (positive logic)



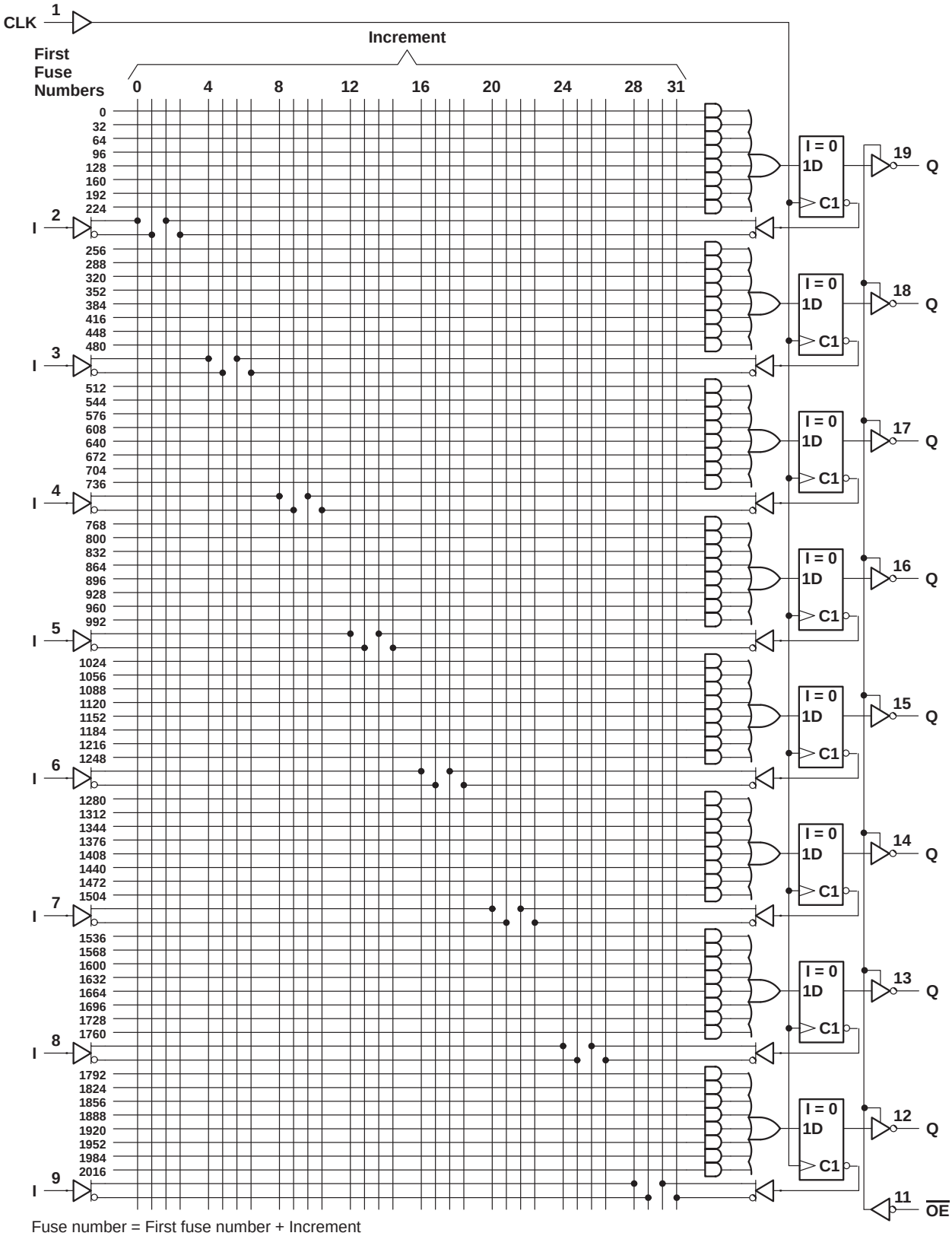
Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range . . . . . –55°C to 125°C
Storage temperature range . . . . . –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–2	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature	–55	25	125	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –2 mA		2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.25	0.4	V
I_{OZH}	Outputs	V_{CC} = 5.5 V,	V_O = 2.7 V				20	μA
	I/O ports						100	
I_{OZL}	Outputs	V_{CC} = 5.5 V,	V_O = 0.4 V				–20	μA
	I/O ports						–100	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V				0.2	mA
I_{IH}	I/O Ports	V_{CC} = 5.5 V,	V_I = 2.7 V				100	μA
	All others						25	
I_{IL}	$\overline{OE}$ input	V_{CC} = 5.5 V,	V_I = 0.4 V				–0.2	mA
	All others						–0.1	
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0.5 V		–30		–250	mA
I_{CC}		V_{CC} = 5.5 V,	V_I = 0,	Outputs open		75	180	mA

timing requirements

			MIN	MAX	UNIT
f_{clock}	Clock Frequency		0	25	MHz
t_w	Pulse duration (see Note 2)	Clock high	15		ns
		Clock low	20		
t_{su}	Setup time, input or feedback before CLK↑		25		ns
t_h	Hold time, input or feedback after CLK↑		0		ns

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock}. The minimum pulse durations specified are only for clock high or low, but not for both simultaneously.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}			R1 = 390 Ω, R2 = 750 Ω, See Figure 1	25	45		MHz
t_{pd}	I, I/O	O, I/O			15	30	ns
t_{pd}	CLK↑	Q			10	20	ns
t_{en}	$\overline{OE}$↓	Q			15	25	ns
t_{dis}	$\overline{OE}$↑	Q			10	25	ns
t_{en}	I, I/O	O, I/O			14	30	ns
t_{dis}	I, I/O	O, I/O			13	30	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment degradation.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –2 mA		2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.25	0.4	V
I_{OZH}	Outputs	V_{CC} = 5.5 V,	V_O = 2.7 V				20	μA
	I/O ports						100	
I_{OZL}	Outputs	V_{CC} = 5.5 V,	V_O = 0.4 V				–20	μA
	I/O ports						–100	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V				0.2	mA
I_{IH}	I/O Ports	V_{CC} = 5.5 V,	V_I = 2.7 V				100	μA
	All others						25	
I_{IL}	$\overline{OE}$ input	V_{CC} = 5.5 V,	V_I = 0.4 V				–0.2	mA
	All others						–0.1	
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0.5 V		–30		–250	mA
I_{CC}		V_{CC} = 5.5 V,	V_I = 0,	Outputs open		75	90	mA

timing requirements

			MIN	MAX	UNIT
f_{clock}	Clock Frequency		0	16	MHz
t_w	Pulse duration (see Note 2)	Clock high	25		ns
		Clock low	25		
t_{su}	Setup time, input or feedback before CLK↑		35		ns
t_h	Hold time, input or feedback after CLK↑		0		ns

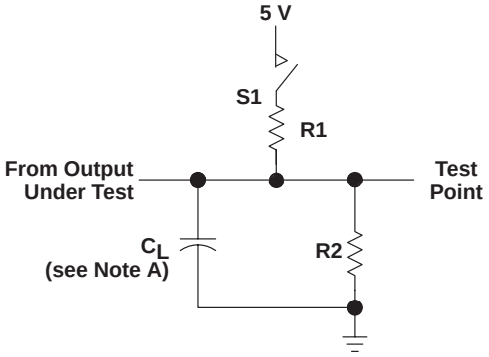
NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock}. The minimum pulse durations specified are only for clock high or low, but not for both simultaneously.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

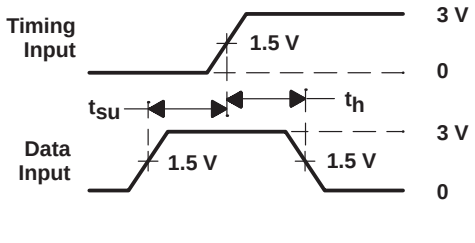
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}			R1 = 390 Ω, R2 = 750 Ω, See Figure 1	16	25		MHz
t_{pd}	I, I/O	O, I/O			25	40	ns
t_{pd}	CLK↑	Q			11	25	ns
t_{en}	$\overline{OE}$↓	Q			20	25	ns
t_{dis}	$\overline{OE}$↑	Q			11	25	ns
t_{en}	I, I/O	O, I/O			25	40	ns
t_{dis}	I, I/O	O, I/O			25	35	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment degradation.

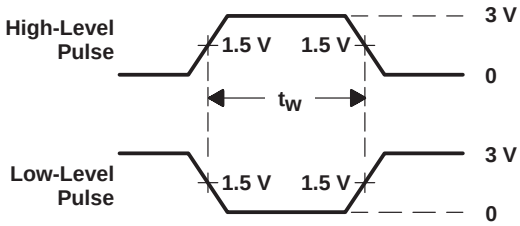
PARAMETER MEASUREMENT INFORMATION



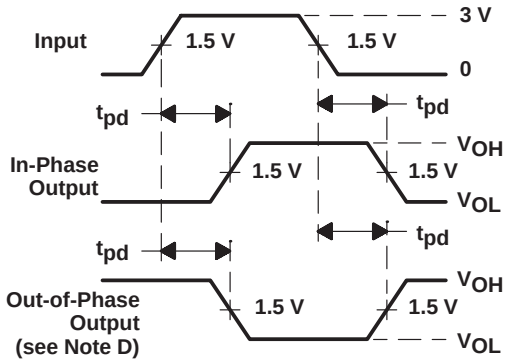
LOAD CIRCUIT FOR 3-STATE OUTPUTS



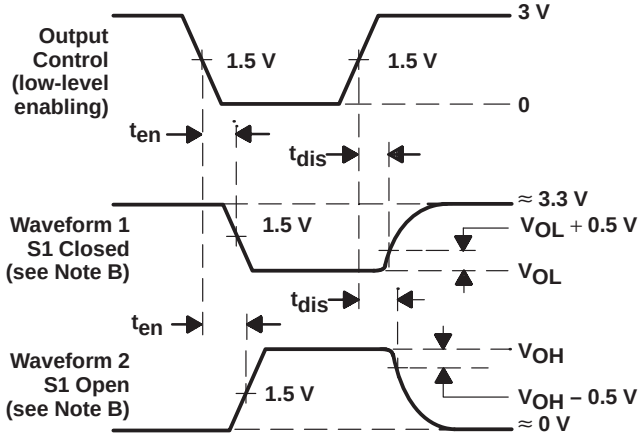
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 10 MHz, t_r and t_f ≤ 2 ns, duty cycle = 50%
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
81036072A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81036072A PAL16L8A MFKB	Samples
8103607RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8103607RA PAL16L8AMJB	Samples
8103607SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8103607SA PAL16L8AMWB	Samples
81036082A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81036082A PAL16R8A MFKB	Samples
8103608RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8103608RA PAL16R8AMJB	Samples
81036092A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81036092A PAL16R6A MFKB	Samples
8103609RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8103609RA PAL16R6AMJB	Samples
81036102A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81036102A PAL16R4A MFKB	Samples
8103610RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8103610RA PAL16R4AMJB	Samples
8103610SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8103610SA PAL16R4AMWB	Samples
81036112A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81036112A PAL16L8A-2MFKB	Samples
8103611RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8103611RA PAL16L8A-2MJB	Samples
81036142A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81036142A PAL16R4A-2MFKB	Samples
PAL16L8A-2MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81036112A PAL16L8A-2MFKB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PAL16L8A-2MJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	PAL16L8A-2MJ	Samples
PAL16L8A-2MJB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8103611RA PAL16L8A-2MJB	Samples
PAL16L8AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81036072A PAL16L8A MFKB	Samples
PAL16L8AMJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	PAL16L8AMJ	Samples
PAL16L8AMJB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8103607RA PAL16L8AMJB	Samples
PAL16L8AMWB	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8103607SA PAL16L8AMWB	Samples
PAL16R4A-2MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81036142A PAL16R4A-2MFKB	Samples
PAL16R4A-2MJ	NRND	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	PAL16R4A-2MJ	
PAL16R4AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81036102A PAL16R4A MFKB	Samples
PAL16R4AMJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	PAL16R4AMJ	Samples
PAL16R4AMJB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8103610RA PAL16R4AMJB	Samples
PAL16R4AMWB	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8103610SA PAL16R4AMWB	Samples
PAL16R6AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81036092A PAL16R6A MFKB	Samples
PAL16R6AMJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	PAL16R6AMJ	Samples
PAL16R6AMJB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8103609RA PAL16R6AMJB	Samples
PAL16R8AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	81036082A PAL16R8A MFKB	Samples
PAL16R8AMJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	PAL16R8AMJ	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PAL16R8AMJB	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8103608RA PAL16R8AMJB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

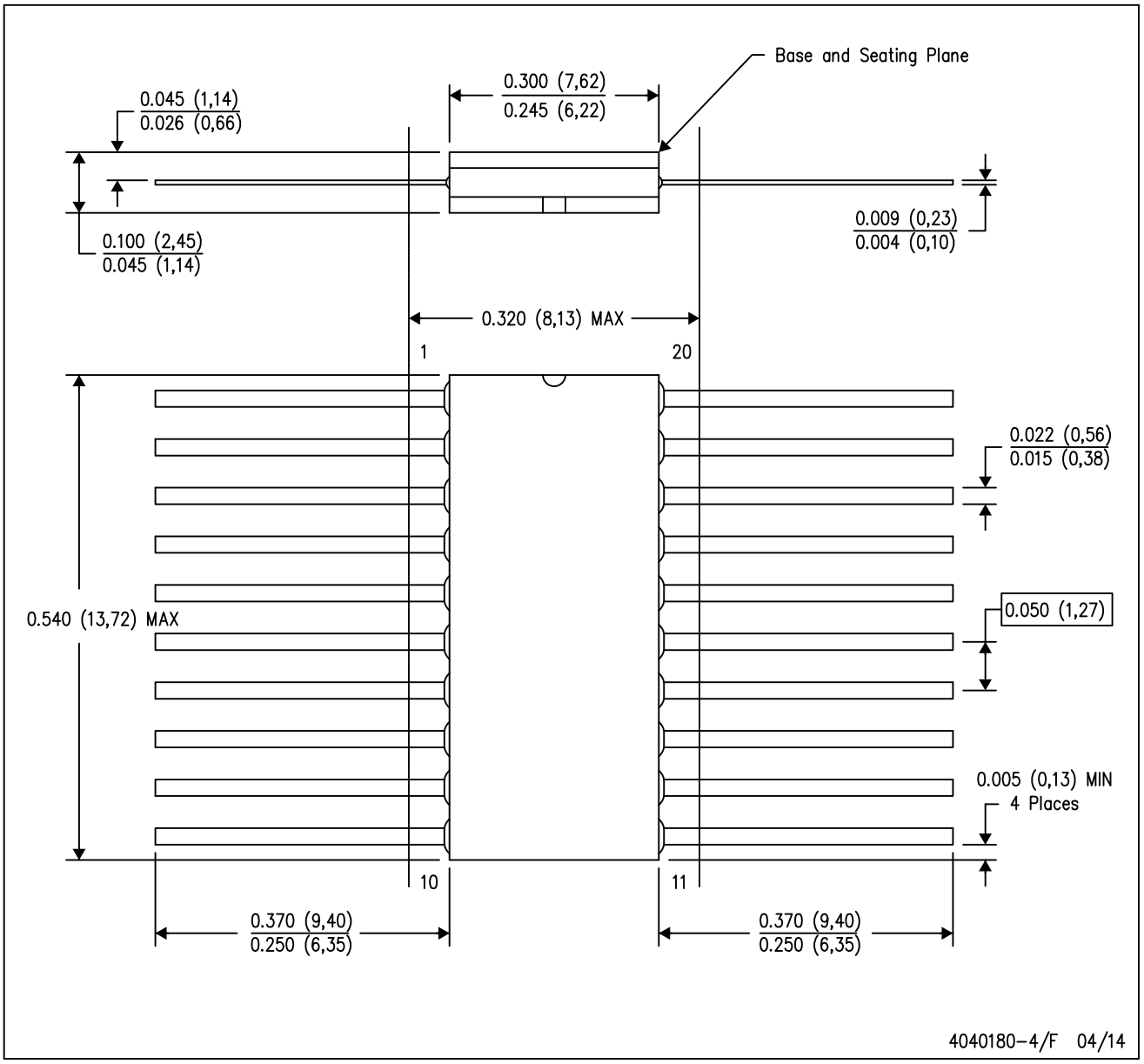
OTHER QUALIFIED VERSIONS OF PAL16L8A-2M, PAL16L8AM, PAL16R4AM, PAL16R6AM, PAL16R8AM :

- Catalog: PAL16L8A-2, PAL16L8A, PAL16R4A, PAL16R6A, PAL16R8A

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

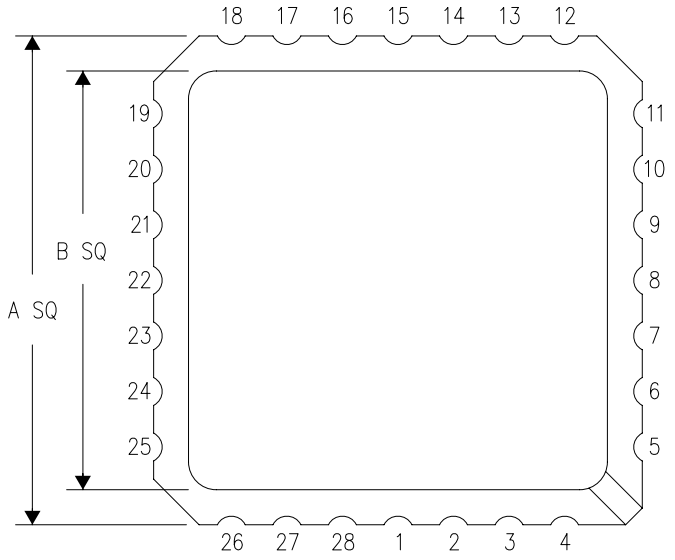
W (R–GDFP–F20) CERAMIC DUAL FLATPACK



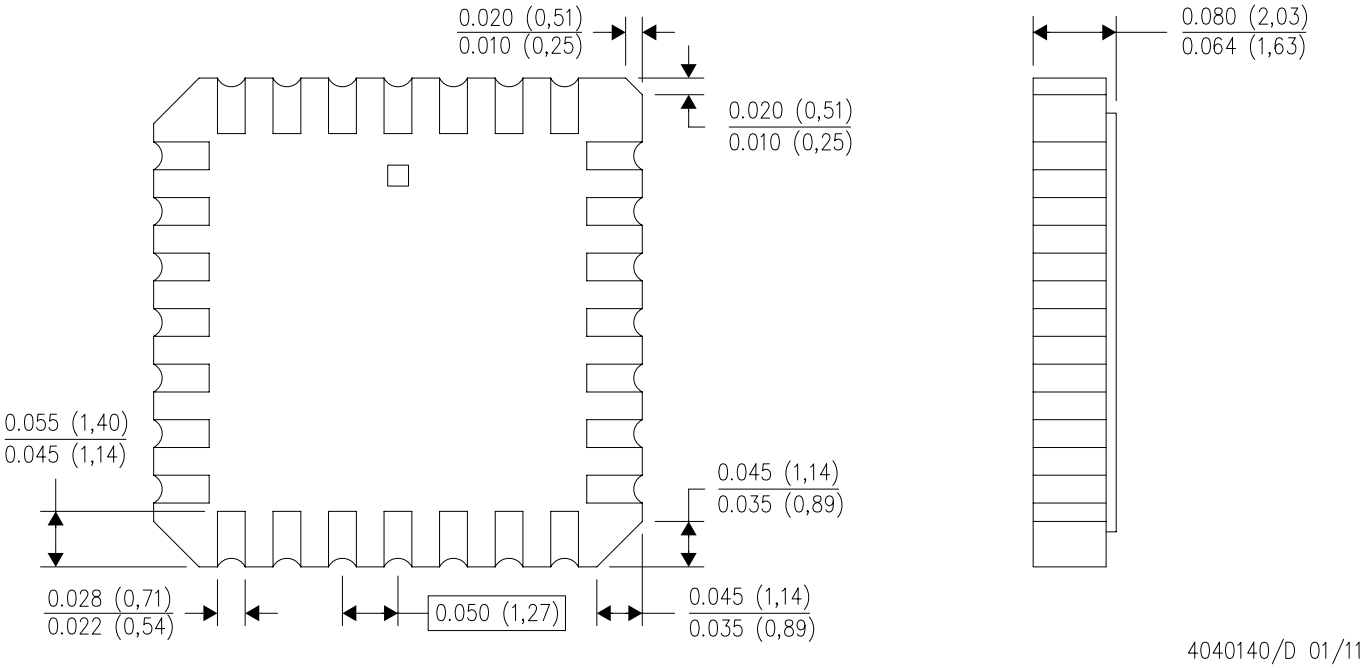
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



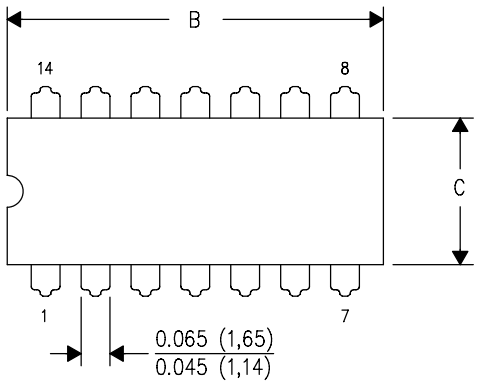
4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

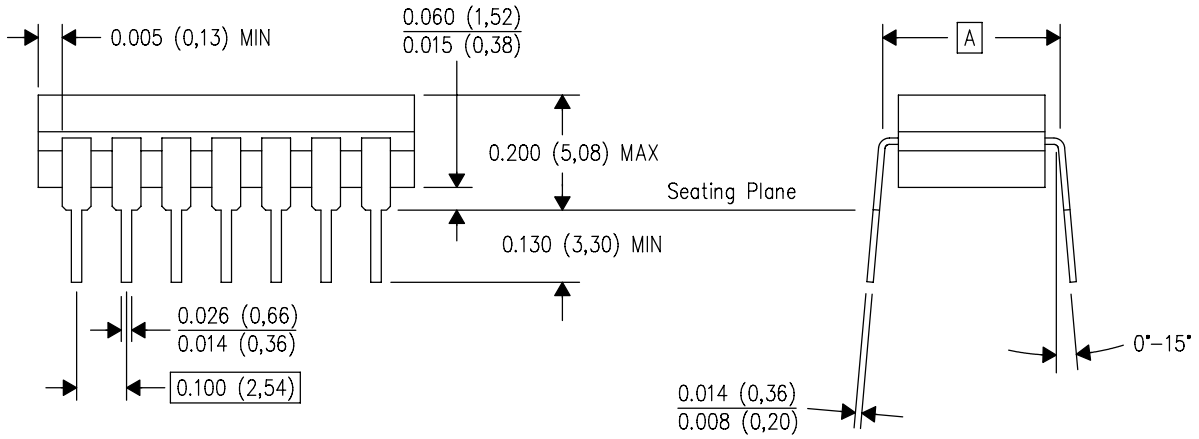
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

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