



IRF9521
R9521

Preliminary

T-37-25



**P-Channel Enhancement-Mode
Vertical DMOS Power FETs**

Ordering Information

BV _{DSS} / BV _{DGS}	R _{DS(ON)} (max)	I _{D(ON)} (min)	Order Number / Package	
			TO-220	TO-92
-60V	0.6Ω	-6.0A	IRF9521	R9521

Features

- Freedom from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain

Advanced DMOS Technology

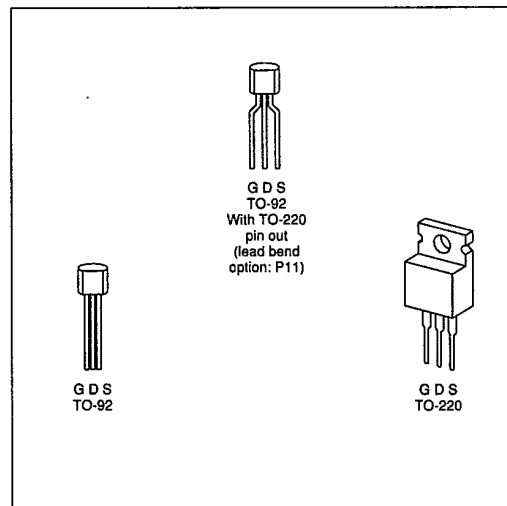
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options



Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ $T_C = 25^\circ\text{C}$	θ_{JC} $^\circ\text{C/W}$	θ_{JA} $^\circ\text{C/W}$	I_{DR}	I_{DRM}^*
IRF9521	-6.0A	-24.0A	40W	80	3.12	-6.0A	-24.0A
R9521	-0.8A	-7.5A	1W	125	170	-0.8A	-7.5A

* I_D (continuous) is limited by max rated T_J .

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Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60			V	$V_{GS} = 0, I_D = -250\mu\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	-2.0		-4.0	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
I_{GSS}	Gate Body Leakage			-500	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = \text{Max Rating}$
I_{DSS}	Zero Gate Voltage Drain Current			-250	μA	$V_{GS} = 0, V_{DS} = \text{Max Rating}$
				-1000		$V_{GS} = 0, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	-6.0			A	$V_{GS} = -10\text{V}$ $V_{DS} > I_{D(ON)} \times R_{DS(ON)} \text{ Max Rating}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			0.8	Ω	$V_{GS} = -10\text{V}, I_D = -3.5\text{A}$
G_{FS}	Forward Transconductance	0.9			S	$V_{DS} > I_{D(ON)} \times R_{DS(ON)} \text{ Max}$ $I_D = -3.5\text{A}$
C_{ISS}	Input Capacitance			450	pF	$V_{GS} = 0\text{V}, V_{DS} = -25\text{V}$ $f = 1 \text{ MHz}$
C_{OSS}	Common Source Output Capacitance			350		
C_{RSS}	Reverse Transfer Capacitance			100		
$t_{d(ON)}$	Turn-ON Delay Time			50	ns	$V_{DD} = 0.5BV_{DSS}$ $I_D = -3.5\text{A}$ $R_S = 50\Omega$
t_r	Rise Time			100		
$t_{d(OFF)}$	Turn-OFF Delay Time			100		
t_f	Fall Time			100		
V_{SD}	Diode Forward Voltage Drop			6.3		
t_{rr}	Reverse Recovery Time		230		ns	$T_J = 150^\circ\text{C}, I_F = -6.0\text{A},$ $di_{F/dt} = 100\text{A}/\mu\text{S}$

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

