MAY 1972 - REVISED MARCH 1988

- Fast Multiplication of Two Binary Numbers 8-Bit Product in 40 ns Typical
- Expandable for N-Bit-by-n-Bit Applications: 16-Bit Product in 70 ns Typical 32-Bit Product in 103 ns Typical
- Fully Compatible with Most TTL Circuits
- Diode-Clamped Inputs Simplify System Design

description

These high-speed TTL circuits are designed to be used in high-performance parallel multiplication applications. When connected as shown in Figure A, these circuits perform the positive-logic multiplication of two 4-bit binary words. The eight-bit binary product is generated with typically only 40 nanoseconds delay.

This basic four-by-four multiplier can be utilized as a fundamental building block for implementing larger multipliers. For example, the four-by-four building blocks can be connected as shown in Figure B to generate submultiple partial products. These results can then be summed in a Wallace tree, and, as illustrated, will produce a 16-bit product for the two eight-bit words typically in 70 nanoseconds. SN54H183/SN74H183 carry-save adders and SN54S181/SN74S181 arithmetic logic units with the SN54S182/SN74S182 look-ahead generator are used to achieve this high performance. The scheme is expandable for implementing N \times M bit multipliers.

The SN54284 and SN54285 are characterized for operation over the full military temperature range of -55° C to 125° C; the SN74284 and SN74285 are characterized for operation from 0°C to 70°C.

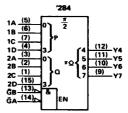
SN54284 . . . J OR W PACKAGE SN74284 . . . N PACKAGE (TOP VIEW)

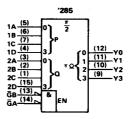
| 2C | D | U_{16} | Vcc |
|-----|-------------|----------|-----|
| 2B | | 15 | 2D |
| 2A | Ľ[3 | 14D | GA |
| 1D | □₄ | 13 | ĞВ |
| 1A | □ 5 | 12 | Y4 |
| 1B | De | - 11 D | Y5 |
| 1C | D7 | 10 | Y6 |
| GND | []8 | ы | ¥7 |

SN54285 . . . J OR W PACKAGE SN74285 . . . N PACKAGE (TOP VIEW)

| 2C | d, | U_{16} | | Vcc |
|-----|-----|----------|---|-----|
| 28 | | 15 | D | 2D |
| 2A | []3 | 14 | | ĞΑ |
| 1D | | 13 | D | ĞΒ |
| 1A | dء | 12 | | Y0 |
| 1B | 6 | 11 | | Y1 |
| 1C | ď٦ | 10 | | Y2 |
| GND | D8 | 9 | D | Y3 |
| | | | | |

logic symbols[†]





[†]These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

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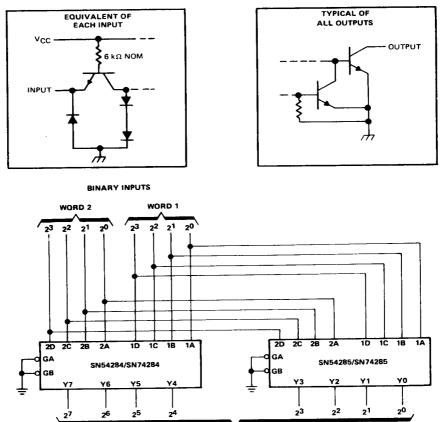
2

ITL Devices

schematics

2

TTL Devices

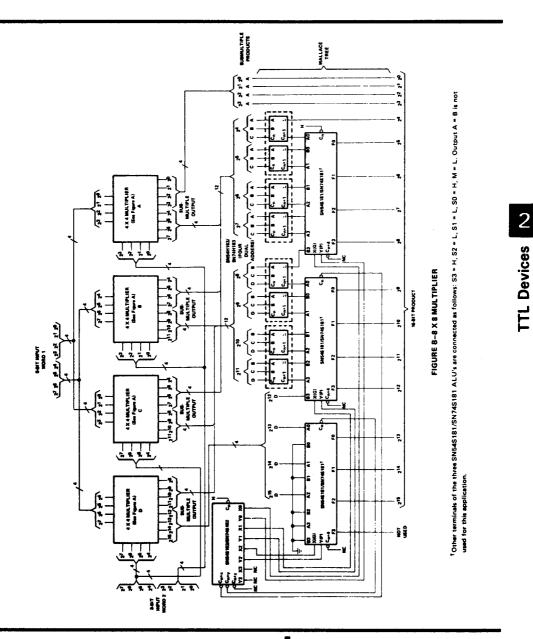


BINARY OUTPUTS

FIGURE A-4 X 4 MULTIPLIER



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| Supply voltage, VCC (see Note 1) | | | | | | | | | | | | | | | | | | 7V |
|---|-------------|------|---|---|---|-----|---|---|---|---|-----|---|---|---|---|---|---|----------------|
| | | | | | | | | | | | | | | | | | | |
| Input voltage Operating free air temperature range | | | | | | | | | | | | | | | | | | |
| | SN74' Circu | its. | | | | | • | • | | • | | • | • | • | • | • | | -0 |
| Storage temperature range | | | • | • | • | • • | · | · | · | • | • • | • | • | | · | · | • | -05 0 10 100 0 |

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

| | | SN5428 | 4 | | UNIT | | |
|------------------------------------|-----|--------|-----|------|------|------|-----|
| | | SN5428 | 5 | : | | | |
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V V |
| Supply voltage, VCC | | | 5.5 | | | 5.5 | V |
| High-level output voltage, VOH | | | 16 | | | 16 | mA |
| Low-level output current, IQL | | | 125 | 0 | | 70 | °C |
| Operating free-air temperature, TA | | | | | | | |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) TANK TYPE MAY LINIT

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| |

| | PARAMETER | TEST CONDITIONS ^T | MIN | TYP | MAX | |
|-----------------|--|---|----------|-----|------|-----|
| | | | 2 | | | V |
| | High-level input voltage | | | | 0.8 | |
| VIL | Low-level input voltage | Vcc = MIN, II = -12 mA | + | | -1.5 | |
| V, | Input clamp voltage | 00 | | | | |
| · · · | | $V_{CC} = MIN, V_{IH} = 2V,$ | | | 40 | μΑ |
| юн | High-level output current | VIL = 0.8 V, VOH = 5.5 V | | | | |
| | | VCC = MIN, IOL = 12 mA | | | 0.4 | 1 1 |
| Voi | | VIH = 2 V, | | | | - v |
| VOL | Low-level output voltage | | | | 0.45 | |
| | | VIL - 0.8 V | + | | | mA |
| h. | Input current at maximum input voltage | V _{CC} = MAX, V _I = 5.5 V | | | | |
| <u> </u> | High-level input current | VCC = MAX, VI = 2.4 V | ļ | | 40 | |
| Чн | | VCC = MAX, V1 = 0.4 V | | | 1 | mA |
| HL. | Low-level input current | West MAY I | 1 | | | |
| | | SN54284, SN54285 | 1 | | 99 | |
| | | T _A = 125°C, N package only | | | | mA |
| 100 | Supply current | See Note 2 | + | | | - 1 |
| 1.00 | | VCC = MAX, SN54284, SN54285 | | 92 | 110 | - 1 |
| ¹ IL | | See Note 2 SN74284, SN74285 | | 92 | 130 | |
| 1 | | | <u> </u> | | | |

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type

 \ddagger All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: With outputs open and both enable inputs grounded, I_{CC} is measured first by selecting an output product which contains three or more high-level bits, then by selecting an output product which contains four low-level bits.

switching characteristics, VCC = 5 V, TA = 25°C

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--------------------------------|-----|-----|-----|------|
| | $C_1 = 30 \text{ pF to GND},$ | | 20 | 30 | |
| tPLH Propagation delay time, low-to-high-level output from enable | $R_{L1} = 300 \Omega$ to VCC, | | 20 | 30 | ns |
| TPHL Propagation delay time, high-to-low-level output from enable | $B_{1,2} = 600 \Omega$ to GND, | | 40 | 60 | 1 |
| TPLH Propagation delay time, low-to-high-level output from word inputs | See Note 3 | | 40 | 60 | ns |
| tPHL Propagation delay time, high-to-low-level output from word inputs | | | | | |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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