



27C64/87C64 64K (8K x 8) CHMOS PRODUCTION AND UV ERASABLE PROMS

- CHMOS Microcontroller and Microprocessor Compatible
 - 87C64-Integrated Address Latch
 - Universal 28 Pin Memory Site, 2-line Control
- Low Power Consumption
 - 100 μ A Maximum Standby Current
- Noise Immunity Features
 - $\pm 10\%$ V_{CC} Tolerance
 - Maximum Latch-up Immunity Through EPI Processing
- High Performance Speeds
 - 150 ns Maximum Access Time
- New Quick-Pulse Programming™ Algorithm (1 second programming)
- Available in 28-Pin Cerdip and Plastic DIP Package and 32-Lead PLCC Package.
 - (See Packaging Spec, Order # 231369)

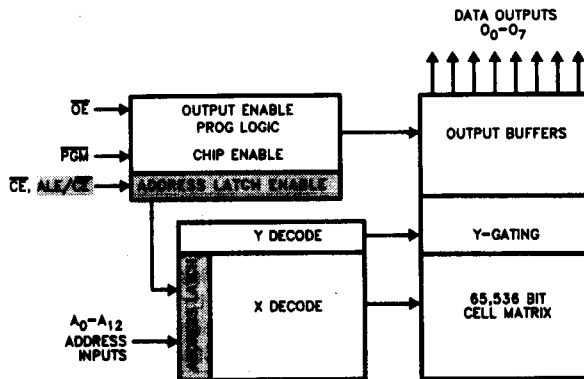
Intel's 27C64 and 87C64 CHMOS EPROMs are 64K bit 5V only memories organized as 8192 words of 8 bits. They employ advanced CHMOS*II-E circuitry for systems requiring low power, high performance speeds, and immunity to noise. The 87C64 has been optimized for multiplexed bus microcontroller and microprocessor compatibility while the 27C64 has a non-multiplexed addressing interface and is plug compatible with the standard Intel 2764A (HMOS II-E).

The 27C64 and 87C64 are offered in both a ceramic DIP, Plastic DIP, and Plastic Leaded Chip Carrier (PLCC) Packages. Cerdip packages provide flexibility in prototyping and R&D environments, whereas Plastic DIP and PLCC EPROMs provide optimum cost effectiveness in production environments. A new Quick-Pulse Programming™ Algorithm is employed which can speed up programming by as much as one hundred times.

The 87C64 incorporates an address latch on the address pins to minimize chip count in multiplexed bus systems. Designers can eliminate an external address latch by tying address and data pins of the 87C64 directly to the processor's multiplexed address/data pins. On the falling edge of the ALE input (ALE/CE), address information at the address inputs (A_0 - A_{12}) of the 87C64 is latched internally. The address inputs are then ignored as data information is passed on the same bus.

The highest degree of protection against latch-up is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins from $-1V$ to $V_{CC} + 1V$.

*HMOS and CHMOS are patented processes of Intel Corporation.



Shaded Areas represent the 87C64 version

Figure 1. Block Diagram

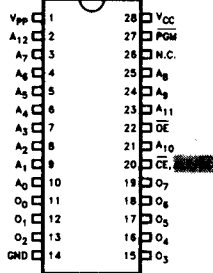
290000-1

Pin Names

A ₀ -A ₁₂	ADDRESSES
O ₀ -O ₇	OUTPUTS
OE	OUTPUT ENABLE
CE	CHIP ENABLE
ALE/CE	ADDRESS LATCH ENABLE / CHIP ENABLE
PGM	PROGRAM STROBE
N.C.	NO CONNECT
D.U.	DON'T USE

27512 27C512	27256 27C256	27128A 27C128	2732A	2716
A ₁₅	V _{PP}	V _{PP}	A ₇	A ₇
A ₁₂	A ₁₂	A ₁₂	A ₆	A ₆
A ₇	A ₇	A ₇	A ₅	A ₅
A ₆	A ₆	A ₆	A ₄	A ₄
A ₅	A ₅	A ₅	A ₃	A ₃
A ₄	A ₄	A ₄	A ₂	A ₂
A ₃	A ₃	A ₃	A ₁	A ₁
A ₂	A ₂	A ₂	A ₀	A ₀
A ₁	A ₁	A ₁	O ₀	O ₀
A ₀	A ₀	A ₀	O ₁	O ₁
O ₀	O ₀	O ₀	O ₂	O ₂
O ₁	O ₁	O ₁	GND	GND
O ₂	O ₂	O ₂		
GND	GND	GND		

27C64/87C64
P27C64/P87C64



2716	2732A	27128A 27C128	27256 27C256	27512 27C512
V _{CC}	V _{CC}	V _{CC} PGM	V _{CC}	V _{CC}
A ₈	A ₈	A ₁₃	A ₁₄	A ₁₄
A ₉	A ₉	A ₈	A ₁₃	A ₁₃
V _{PP}	A ₁₁	A ₉	A ₈	A ₈
OE	OE/V _{PP}	A ₁₁	A ₉	A ₉
A ₁₀	A ₁₀	A ₁₁	A ₁₁	A ₁₁
CE	CE	OE	OE	OE/V _{PP}
O ₇	O ₇	A ₁₀	A ₁₀	A ₁₀
O ₆	O ₆	CE	CE	CE
O ₅	O ₅	O ₇	O ₇	O ₇
O ₄	O ₄	O ₆	O ₆	O ₆
O ₃	O ₃	O ₅	O ₅	O ₅
		O ₄	O ₄	O ₄
		O ₃	O ₃	O ₃

290000-2

NOTE:

Intel "Universal Site" Compatible EPROM Pin Configurations are shown in the adjacent blocks to 27C64 Pins.

Shaded Areas represent the 87C64 version

Figure 2. Pin Configuration

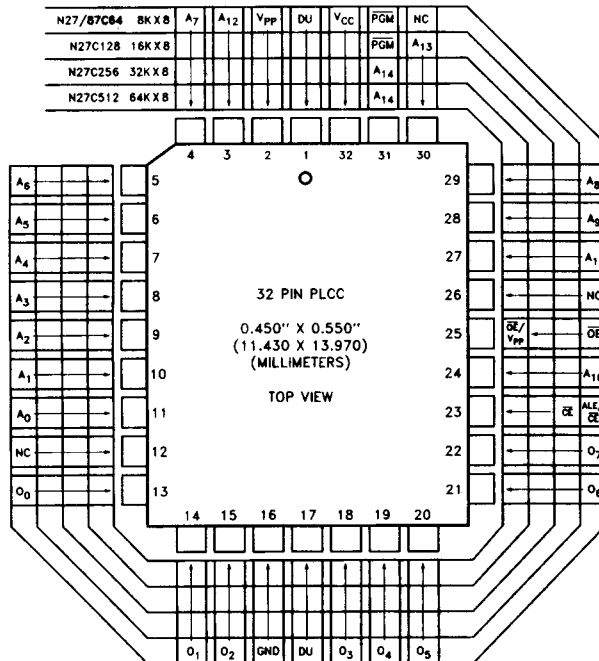


Figure 3. PLCC(N) Lead Configuration

290000-11

Extended Temperature (Express) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications.

EXPRESS EPROM products are available with 168 ± 8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (-40°C to +85°C) EXPRESS products are also available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

READ OPERATION

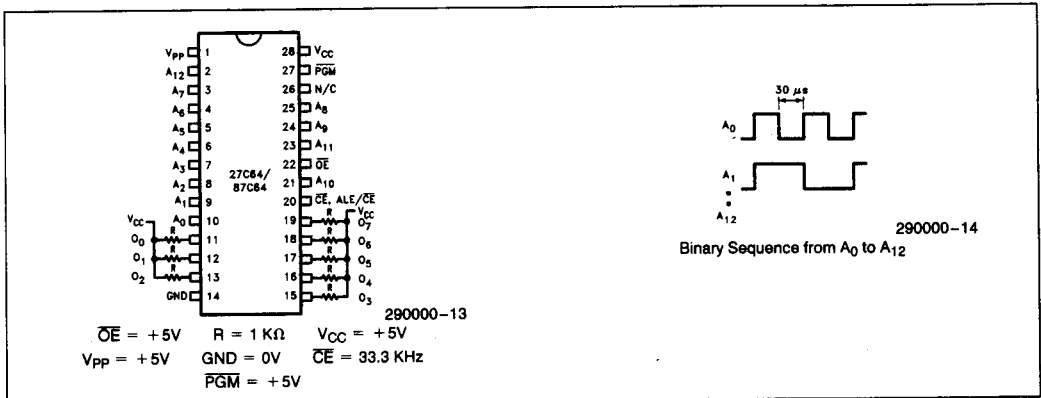
D.C. CHARACTERISTICS

Electrical Parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for:

Symbol	Parameter	27C64 87C64		Test Conditions
		Min	Max	
I _{SB}	V _{CC} Standby Current (mA)	CMOS	0.1	$\overline{OE} = V_{CC}, \overline{OE} = V_{IL}$
		TTL	1.0	$\overline{OE} = V_{IH}, \overline{OE} = V_{IL}$
I _{CC1} ⁽¹⁾	V _{CC} Active Current (mA)	TTL	20, 30	$\overline{OE} = \overline{CE} = V_{IL}$
	V _{CC} Active Current at High Temperature	TTL	20, 30	$\overline{OE} = \overline{CE} = V_{IL}$ $V_{PP} = V_{CC}, T_{ambient} = 85^{\circ}C$

NOTE:

1. See notes 4 and 6 of Read Operation D.C. Characteristics.



EXPRESS EPROM Product Family

PRODUCT DEFINITIONS

Type	Operating Temperature (°C)	Burn-in 125°C (hr)
Q	0 to +70	168 ± 8
T	-40 to +85	NONE
L	-40 to +85	168 ± 8

EXPRESS Options

27C64/87C64 Versions

Packaging Options		
Speed Versions	Cerdip	PLCC
-1	Q (27)	
-20	T, L, Q	T

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	
During Read	0°C to +70°C(2)
Temperature Under Bias	-10°C to +80°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to 7V(1)
Voltage on Pin A ₉ with Respect to Ground	-2.0V to +13.5V(1)
V _{PP} Supply Voltage with Respect to Ground During Programming	-2.0V to +14V(1)
V _{CC} Supply Voltage with Respect to Ground	-2.0V to +7.0V(1)

*Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION D.C. CHARACTERISTICS 0°C ≤ T_A ≤ +70°C

Symbol	Parameter	Notes	Min	Typ(3)	Max	Unit	Test Condition
I _{IL}	Input Leakage Current			0.01	1.0	μA	V _{IN} = 0V to V _{CC}
I _{LO}	Output Leakage Current				±10	μA	V _{OUT} = 0V to V _{CC}
I _{PP1}	V _{PP} Current Read	6			100	μA	V _{PP} = V _{CC}
I _{SB}	V _{CC} Current Standby with Inputs—	CMOS	5		100	μA	CE = V _{CC}
		TTL	4		1.0	mA	CE = V _{IH}
I _{CC1}	V _{CC} Current Active	4, 6			20, 30	mA	CE = V _{IL} f = 5 MHz, I _{OUT} = 0 mA
V _{IL}	Input Low Voltage (±10% Supply) (TTL)		-0.5		0.8	V	V _{PP} = V _{CC}
	Input Low Voltage (CMOS)		-0.2		0.2		
V _{IH}	Input High Voltage (±10% Supply) (TTL)		2.0		V _{CC} + 0.5	V	V _{PP} = V _{CC}
	Input High Voltage (CMOS)		V _{CC} - 0.2		V _{CC} + 0.2		
V _{OL}	Output Low Voltage				0.45	V	I _{OL} = 2.1 mA
V _{OH}	Output High Voltage		3.5			V	I _{OH} = -2.5 mA
I _{OS}	Output Short Circuit Current	7			100	mA	
V _{PP}	V _{PP} Read Voltage	8	V _{CC} - 0.7		V _{CC}	V	

NOTES:

- Minimum D.C. input voltage is -0.5V. During transitions, the inputs may undershoot to -2.0V for periods less than 20 ns. Maximum D.C. Voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2V for periods less than 20 ns.
- Operating temperature is for commercial product defined by this specification. Extended temperature options are available in EXPRESS and Military version.
- Typical limits are at V_{CC} = 5V, T_A = +25°C.
- 20 mA for STD and -3 versions; 30 mA for -2 and 150 ns versions.

V_{IL}, V_{IH} levels at TTL inputs.

5. ALE/CE or CE is V_{CC} ± 0.2V. All other inputs can have any value within spec.

6. Maximum Active power usage is the sum I_{PP} + I_{CC}. The maximum current value is with Outputs O₀ to O₇ unloaded.

7. Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.

8. V_{PP} may be one diode voltage drop below V_{CC}. It may be connected directly to V_{CC}.

READ OPERATION

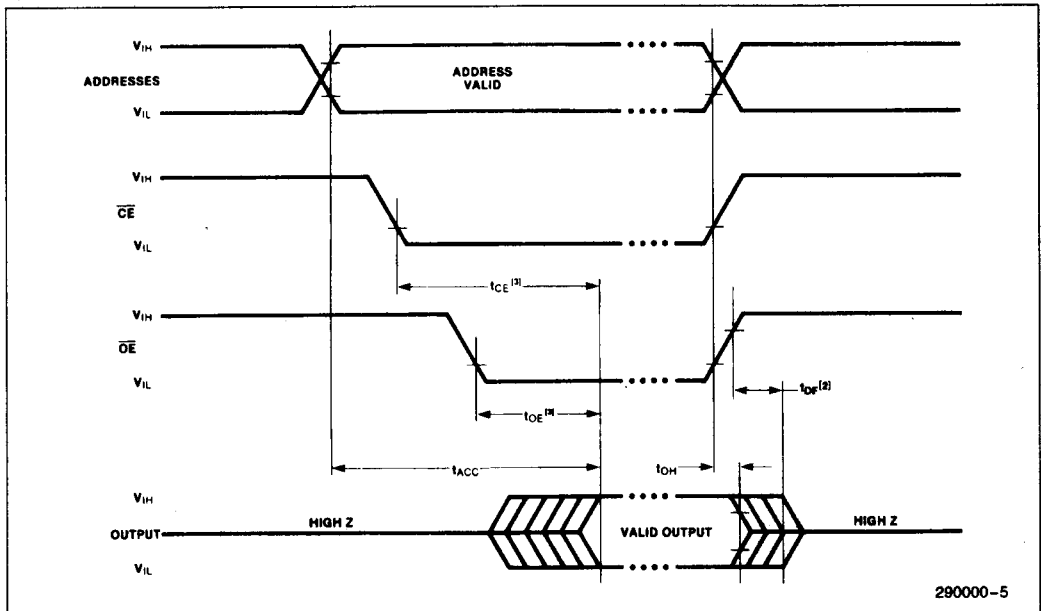
A.C. CHARACTERISTICS 27C64⁽¹⁾ 0°C ≤ T_A ≤ +70°C

Versions (3)		V _{CC} ± 5%	27C64-1 N27C64-1 P27C64-1		27C64-2 N27C64-2 P27C64-2		27C64 N27C64		Unit
		V _{CC} ± 10%	27C64-15 N27C64-15		27C64-20 N27C64-20 P27C64-20		27C64-25		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max		
t _{ACC}	Address to Output Delay		150		200		250	ns	
t _{CE}	\overline{CE} to Output Delay		150		200		250	ns	
t _{OE}	\overline{OE} to Output Delay		75		75		100	ns	
t _{DF} ⁽²⁾	\overline{OE} High to Output High Z		35		55		60	ns	
t _{OH} ⁽²⁾	Output Hold from Addresses, \overline{CE} or \overline{OE} Change-Whichever is First	0		0		0		ns	

NOTES:

- A.C. characteristics tested at V_{IH} = 2.4V and V_{IL} = 0.45V.
Timing measurements made at V_{OL} = 0.8V and V_{OH} = 2.0V.
- Guaranteed and sampled.
- Model Number Prefixes: No prefix = Cerdip; P = Plastic DIP; N = PLCC.

A.C. WAVEFORMS 27C64



NOTES:

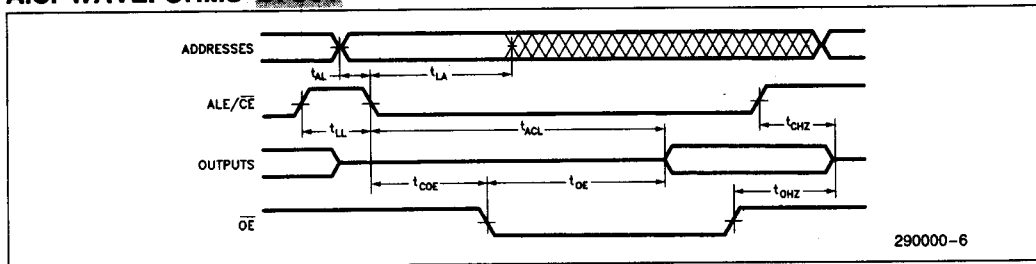
- Typical values are for T_A = 25°C and nominal supply voltages.
- This parameter is only sampled and is not 100% tested.
- \overline{OE} may be delayed up to t_{CE}-t_{OE} after the falling edge of \overline{CE} without impact on t_{CE}.

A.C. CHARACTERISTICS 87C64(1) $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$

Versions (3)	Parameter	$V_{CC} \pm 5\%$		87C64-2 N87C64-2		87C64 N87C64		Unit
		$V_{CC} \pm 10\%$		87C64-20 N87C64-20		87C64-25 N87C64-25		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	
t_{LL}	Chip Deselect Width	50		50		60		ns
t_{AL}	Address to \overline{CE} -Latch Set-up	7		20		25		ns
t_{LA}	Address Hold from \overline{CE} -LATCH	30		45		50		ns
t_{ACL}	\overline{CE} -Latch Access Time		150		200		250	ns
t_{OE}	Output Enable to Output Valid		75		75		100	ns
t_{COE}	ALE/ \overline{CE} to Output Enable	30		45		50		ns
$t_{CHZ}^{(2)}$	Chip Deselect to Output in High Z		45		50		60	ns
$t_{OHZ}^{(2)}$	Output Disable to Output in High Z		35		50		60	ns

NOTES:

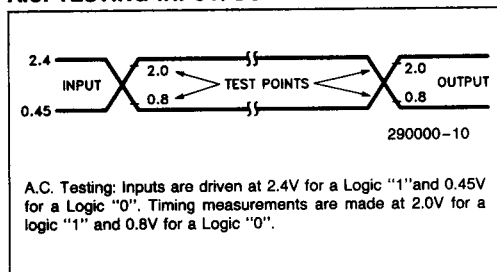
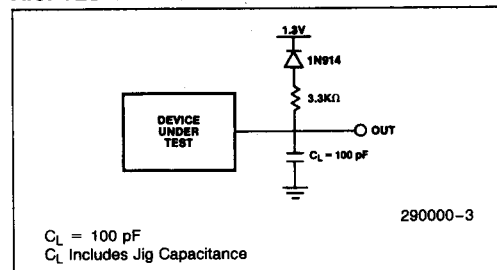
- A.C. characteristics tested at $V_{IH} = 2.4\text{V}$ and $V_{IL} = 0.45\text{V}$.
Timing measurements made at $V_{OL} = 0.8\text{V}$ and $V_{OH} = 2.0\text{V}$.
- Guaranteed and sampled.
- Model Number Prefixes: No prefix = Cerdip; N = PLCC.

A.C. WAVEFORMS 87C64

CAPACITANCE(1) $T_A = 25^{\circ}\text{C}$, $f = 1.0\text{ MHz}$

Symbol	Parameter	Max	Unit	Conditions
C_{IN}	Address/Control Capacitance	6	pF	$V_{IN} = 0\text{V}$
C_{OUT}	Output Capacitance	12	pF	$V_{OUT} = 0\text{V}$

NOTE:

- Sampled. Not 100% tested.

A.C. TESTING INPUT/OUTPUT WAVEFORM

A.C. TESTING LOAD CIRCUIT


DEVICE OPERATION

The modes of operation of the 27C64/87C64 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for intelligent Identifier mode.

Table 1. Mode Selection for 27C64 and 87C64

Pins	ALE CE	OE	PGM (7)	A_9	A_0	V_{PP} (7)	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	X ⁽¹⁾	X	V_{CC}	5.0V	D _{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	X	X	X	V_{CC}	5.0V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	X	X	(4)	(4)	D _{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	X	X	(4)	(4)	D _{OUT}
Program Inhibit	V_{IH}	X	X	X	X	(4)	(4)	HIGH Z
intelligent Identifier ⁽³⁾ -Manufacturer	V_{IL}	V_{IL}	V_{IH}	V_H ⁽²⁾	V_{IL}	V_{CC}	V_{CC}	89 H (6) 88 H (6)
intelligent Identifier ⁽³⁾ -27C64	V_{IL}	V_{IL}	V_{IH}	V_H ⁽²⁾	V_{IH}	V_{CC}	V_{CC}	07 H
intelligent Identifier ^(3, 5) -87C64	V_{IL}	V_{IL}	V_{IH}	V_H ⁽²⁾	V_{IH}	V_{CC}	V_{CC}	37 H

NOTES:

- X can be V_{IL} or V_{IH} .
- $V_H = 12.0V \pm 0.5V$.
- $A_1-A_8, A_{10-12} = V_{IL}$.
- See Table 2 for V_{CC} and V_{PP} voltages.
- ALE/ \overline{CE} has to be toggled in order to latch in the addresses and read the signature codes.
- The Manufacturer's identifier reads 89H for Cerdip devices; 88H for Plastic DIP and PLCC devices.
- In Read Mode tie PGM and V_{PP} to V_{CC} .

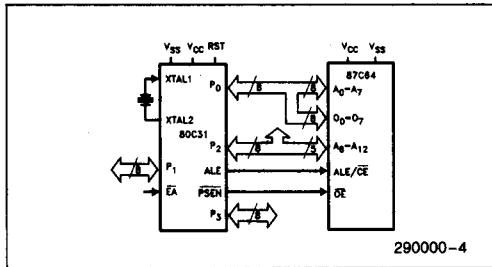
Read Mode: 27C64

The 27C64 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (\overline{CE}) is the power control and should be used for device selection. Output enable (\overline{OE}) is the output control and should be used to gate data from the output pins. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from \overline{CE} to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of \overline{OE} , assuming that \overline{CE} has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Read Mode: 87C64

The 87C64 was designed to reduce the hardware interface requirements when incorporated in processor systems with multiplexed address-data busses. Chip count (and therefore power and board space) can be minimized when the 87C64 is designed as shown in Figure 4. The processor's multiplexed bus (AD_{0-7}) is tied to both address and data pins of the 87C64. All address inputs of the 87C64 are latched when ALE/ \overline{CE} is brought low, thus eliminating the need for a separate address latch.

The 87C64 internal address latch is directly enabled through the use of the ALE/ \overline{CE} line. As the transition occurs on the ALE/ \overline{CE} from the TTL high to the low state, the last address presented at the address pins is retained. Data is then enabled onto the bus from the EPROM by the \overline{OE} pin.



**Figure 4. 80C31 with 87C64
System Configuration**

Standby Mode

The 27C64 and 87C64 have Standby modes which reduce the maximum V_{CC} current to 100 μA . Both are placed in the Standby mode when \overline{CE} or ALE/ \overline{CE} are in the CMOS-high state. When in the Standby mode, the outputs are in a high impedance state, independent of the \overline{OE} input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

- the lowest possible memory power dissipation, and
- complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, \overline{CE} (or ALE/ \overline{CE}) should be decoded and used as the primary device selecting function, while \overline{OE} should be made a common connection to all devices in the array and connected to the \overline{READ} line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC} , has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient and inductive current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor for low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The device is in the programming mode when V_{PP} is raised to its programming voltage (See Table 2) and \overline{CE} (or ALE/ \overline{CE}) and PGM are both at TTL low and $\overline{OE} = V_{IH}$. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level \overline{CE} (or ALE/ \overline{CE}) or PGM input inhibits the other devices from being programmed.

Except for \overline{CE} (or ALE/\overline{CE}), all like inputs (including \overline{OE}) of the parallel EPROMs may be common. A TTL low-level pulse applied to the PGM input with V_{PP} at its programming voltage and \overline{CE} (or ALE/\overline{CE}) = V_{IL} will program the selected device.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with \overline{OE} and \overline{CE} (or ALE/\overline{CE}) at V_{IL} , PGM at V_{IH} , and V_{CC} and V_{PP} at their programming voltages. Data should be verified a minimum of t_{OE} after the falling edge of \overline{OE} .

intelligent Identifier™ Mode

The intelligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH} . All other address lines must be held at V_{IL} during the intelligent Identifier Mode.

Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. These two identifier bytes are given in Table 1. ALE/\overline{CE} of the 87C64 has to be toggled in order to latch in the addresses and read the Signature Codes.

ERASURE CHARACTERISTICS (FOR Cerdip EPROMs)

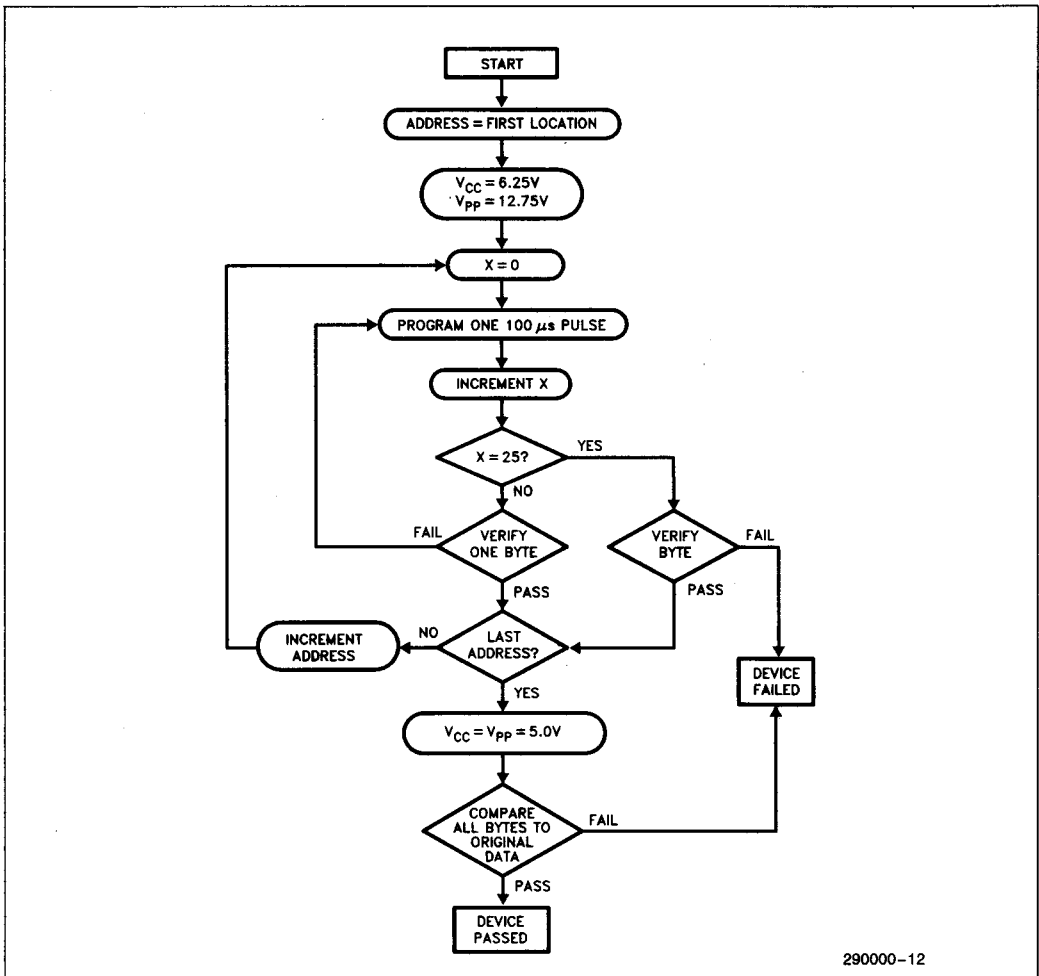
The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (\AA). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 \AA range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (\AA). The integrated dose (i.e., UV intensity \times exposure time) for erasure should be a minimum of 15 Wsec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 $\mu\text{W}/\text{cm}^2$ power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm² (1 week @ 12000 $\mu\text{W}/\text{cm}^2$). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

CHMOS NOISE CHARACTERISTICS

Special EPI processing techniques have enabled Intel to build CHMOS with features adding to system reliability. These include input/output protection to latch-up. Each of the data and address pins will not latch-up with currents up to 100 mA and voltages from -1V to $V_{CC} + 1\text{V}$.

Additionally, the V_{PP} (programming) pin is designed to resist latch-up to the 14V maximum device limit.



290000-12

Figure 5. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm

Intel's 27C64 and 87C64 EPROMs can now be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production environment. This algorithm allows these devices to be programmed in under one second, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte veri-

fication to determine when the address byte has been successfully programmed. Up to 25 100 μ s pulses per byte are provided before a failure is recognized. A flowchart of the Quick-Pulse Programming Algorithm is shown in Figure 5.

For the Quick Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at $V_{CC} = 6.25V$ and $V_{PP} = 12.75V$. When programming of the EPROM has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5.0V$.

D.C. PROGRAMMING CHARACTERISTICS (27C64/87C64) $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$

Table 2

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		1.0	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	-0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1\text{ mA}$
V_{OH}	Output High Voltage During Verify	3.5		V	$I_{OH} = -2.5\text{ mA}$
$I_{CC2}^{(3)}$	V_{CC} Supply Current		30	mA	
$I_{PP2}^{(3)}$	V_{PP} Supply Current (Program)		30	mA	$\overline{CE} = V_{IL}$
V_{ID}	A_9 intelligent Identifier Voltage	11.5	12.5	V	
V_{PP}	Programming Voltage	12.5	13.0	V	
V_{CC}	Supply Voltage During Programming	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS 27C64
 $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$, See Table 2 for V_{CC} and V_{PP} Voltages

Symbol	Parameter	Limits				Conditions (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			μs	
t_{OES}	\overline{OE} Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DFP}	\overline{OE} High to Output Float Delay	0		130	ns	(Note 2)
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{CES}	\overline{CE} Setup Time	2			μs	
t_{PW}	\overline{PGM} Program Pulse Width	95	100	105	μs	Quick-Pulse
t_{OE}	Data Valid from \overline{OE}			150	ns	

A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) 20 ns

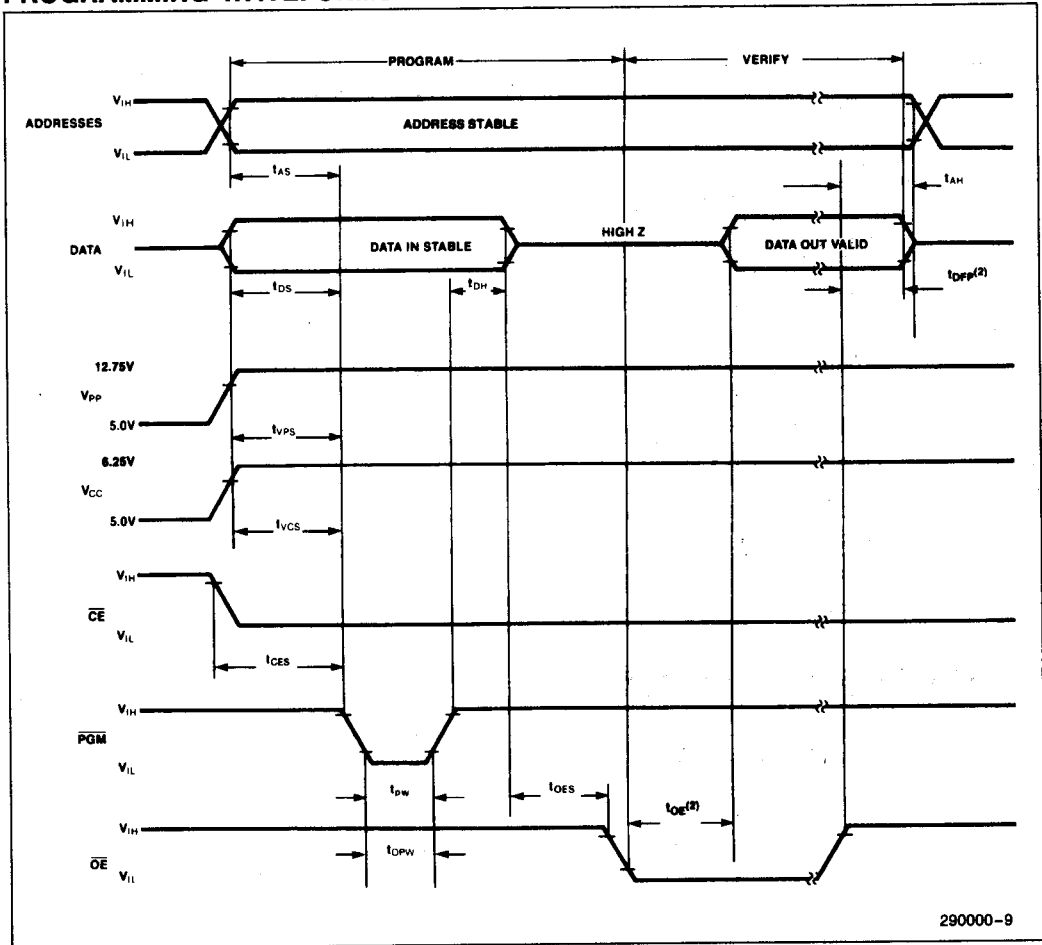
Input Pulse Levels 0.45V to 2.4V

Input Timing Reference Level 0.8V and 2.0V

Output Timing Reference Level 0.8V and 3.5V

NOTES:

- V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .
- This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
- The maximum current value is with outputs O_0 to O_7 Unloaded.

PROGRAMMING WAVEFORMS 27C64


290000-9

NOTES:

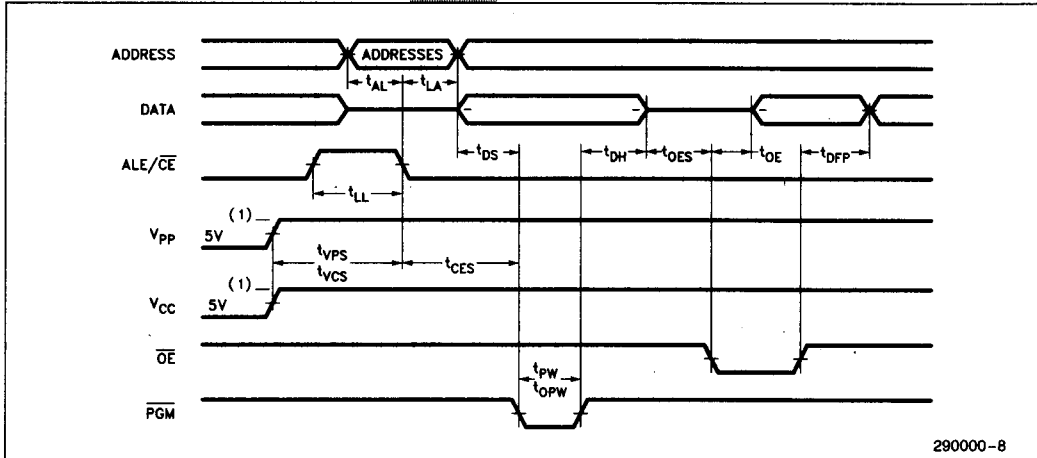
1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27C64, a 0.1 μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

A.C. PROGRAMMING CHARACTERISTICS
 $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$, See Table 2 for V_{CC} and V_{PP} Voltages.

Symbol	Parameter	Limits			Unit	Conditions
		Min	Typ	Max		
t_{VPS}	V_{PP} Setup Time	2			μs	
t_{VCS}	V_{CC} Setup Time	2			μs	
t_{LL}	Chip Deselect Width	2			μs	
t_{AL}	Address to Chip Select Setup	1			μs	
t_{LA}	Address Hold from Chip Select	1			μs	
t_{PW}	$\overline{\text{PGM}}$ Pulse Width	95	100	105	μs	Quick-Pulse
t_{DS}	Data Setup Time	2			μs	
t_{DFP}	$\overline{\text{OE}}$ High to Data Float	0		130	ns	
t_{OES}	Output Enable Setup Time	2			μs	
t_{OE}	Data Valid from Output Enable			150	ns	
t_{DH}	Data Hold Time	2			μs	
t_{CES}	$\overline{\text{CE}}$ Setup Time	2			μs	

NOTE:

1. Programming tolerances and test conditions are the same as 27C64.

PROGRAMMING WAVEFORMS

NOTE:

 1. 12.75V V_{PP} & 6.25V V_{CC} for Quick-Pulse Programming Algorithm.

REVISION HISTORY

Number	Description
09	Revised DIP and PLCC pin configurations. Revised Express options. Deleted -3 and -30 speed bins. Deleted Plastic DIP 87C64 Option.