MOTOROLA

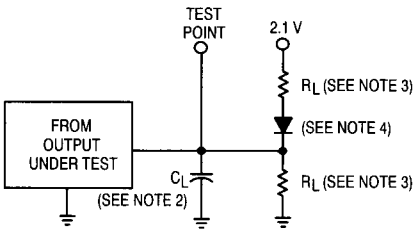
Quad 2-Input Data Selector/Multiplexer 3-State Outputs with Enable

ELECTRICALLY TESTED PER:
MIL-M-38510/30907

The 54LS258A is a Quad 2-Input Multiplexers with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with HIGH on the common Output Enable ($\overline{EO}$) Input, allowing the outputs to interface directly with the bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Schottky Process For High-Speed
- Multiplexer Expansion By Tying Outputs Together
- Non-Inverting 3-State Outputs
- Input Clamp Diodes Limit High-Speed Termination Effects

LOAD CIRCUIT FOR 3-STATE OUTPUT



TRUTH TABLE				
Output Enable	Select Input	Data Inputs		Output
$\overline{EO}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z) = High Impedance

Military 54LS258A

AVAILABLE AS:

1) JAN: JM38510/30907BXA
2) SMD: 7603801
3) 883: 54LS258A/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
S	1	1	2	V_{CC}
I_{0a}	2	2	3	V_{CC}
I_{1a}	3	3	4	V_{CC}
$\overline{Z}_a$	4	4	5	OPEN
I_{0b}	5	5	7	V_{CC}
I_{1b}	6	6	8	V_{CC}
$\overline{Z}_b$	7	7	9	OPEN
GND	8	8	10	GND
$\overline{Z}_d$	9	9	12	OPEN
I_{1d}	10	10	13	V_{CC}
I_{0d}	11	11	14	V_{CC}
$\overline{Z}_c$	12	12	15	OPEN
I_{1c}	13	13	17	V_{CC}
I_{0c}	14	14	18	V_{CC}
$\overline{EO}$	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

NOTES:
1. Input pulse characteristics: PRR ≤ 1.0 MHz, t_r = 15 ns, t_f ≤ 6.0 ns.
2. C_L = 50 pF ± 10% for t_{PLH}, t_{PHL}, t_{PZL} and t_{PZH} tests, C_L = 15 pF minimum for t_{PHZ} and t_{PLZ} tests. C_L includes scope probe, wiring and stray capacitance.
3. R_L = 2.0 kΩ ± 5.0%.
4. All diodes are 1N3064 or 1N916.
5. The limits specified for C_L = 15 pF, guaranteed but not tested.

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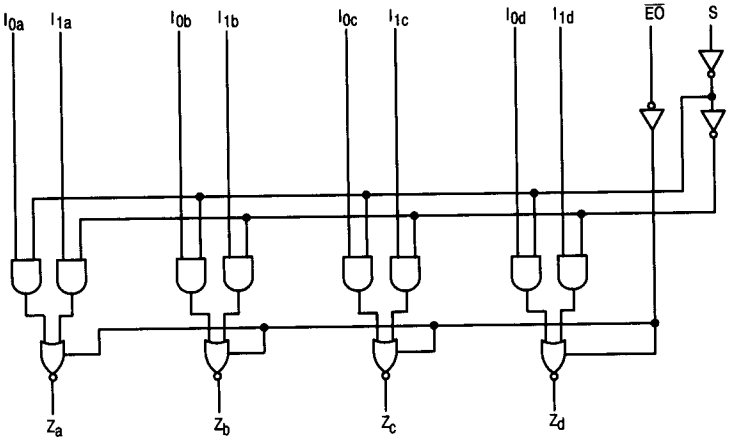
FUNCTIONAL DESCRIPTION

The 'LS258A is a Quad 2-Input Multiplexer with 3-state outputs. It selects four bits of data from two sources under the control of a Common Data Select input. When the Select input is LOW, the I_0 inputs are selected and when Select is HIGH, I_1 inputs are selected. The data on the selected inputs appears at the outputs in the inverted form for the 'LS258A. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown:

$$Z_a = \overline{EO} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \quad Z_b = \overline{EO} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$Z_c = \overline{EO} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \quad Z_d = \overline{EO} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

When the Output Enable Input (EO) is HIGH, the outputs are forced to a high impedance "Off" state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

LOGIC DIAGRAM



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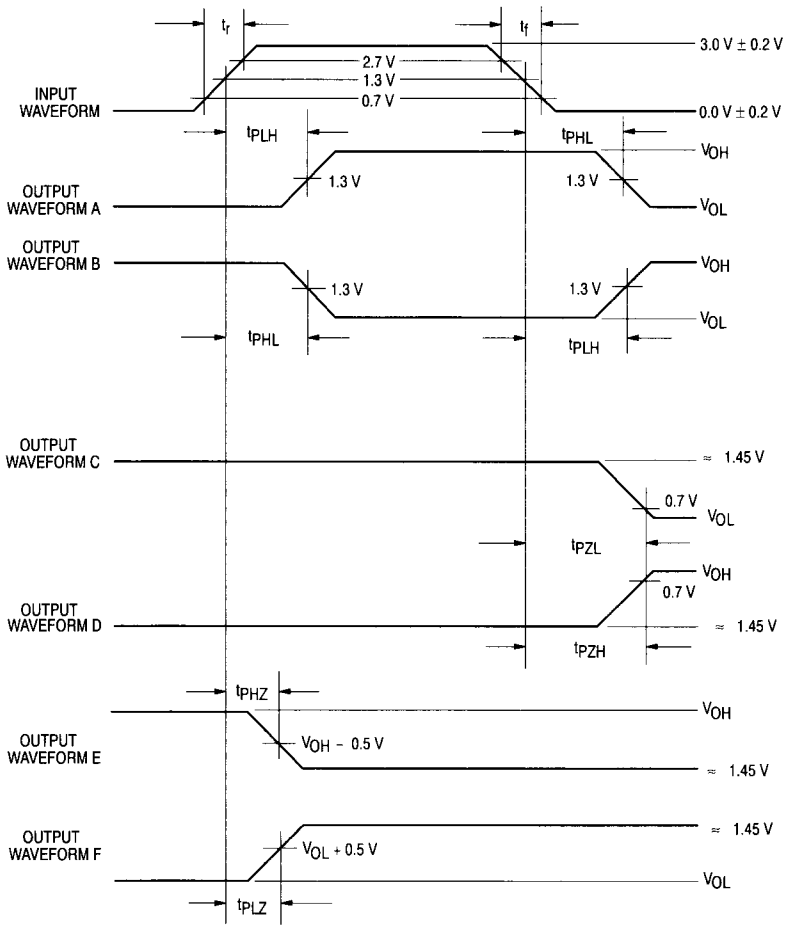
WAVEFORMS


t_r
t_f
3.0 V ± 0.2 V
2.7 V
1.3 V
0.7 V
INPUT WAVEFORM
0.0 V ± 0.2 V
t_{PLH}
t_{PHL}
V_{OH}
1.3 V
1.3 V
OUTPUT WAVEFORM A
V_{OL}
OUTPUT WAVEFORM B
V_{OH}
1.3 V
1.3 V
V_{OL}
t_{PHL}
t_{PLH}
OUTPUT WAVEFORM C
≈ 1.45 V
0.7 V
V_{OL}
t_{PZL}
V_{OH}
0.7 V
OUTPUT WAVEFORM D
≈ 1.45 V
t_{PZH}
t_{PHZ}
V_{OH}
OUTPUT WAVEFORM E
V_{OH} - 0.5 V
≈ 1.45 V
OUTPUT WAVEFORM F
≈ 1.45 V
V_{OL} + 0.5 V
V_{OL}
t_{PLZ}

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = − 1.0 mA, V_{IL} = 0.7 V, S = 0.7 V, $\overline{EO}$ = 0.7 V, other inputs are open.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 12 mA, V_{IH} = 2.0 V, S = 2.0 V, $\overline{EO}$ = 0.7 V, other inputs are open.
V_{IC}	Input Clamping Voltage		− 1.5					V	V_{CC} = 4.5 V, I_{IN} = − 18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open, S = 5.5 V or GND.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open, S = 5.5 V or GND.
$I_{IH(S)}$	Logical "1" Input Current		40		40		40	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
$I_{IHH(S)}$	Logical "1" Input Current		200		200		200	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, other inputs are open.
I_{IL}	Logical "0" Input Current	− 0.16	− 0.4	− 0.16	− 0.4	−0.16	− 0.4	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs are open, S = 5.5 V or GND.
$I_{IL(S)}$	Logical "0" Input Current	− 0.25	− 0.7	− 0.25	− 0.7	− 0.25	− 0.7	mA	V_{CC} = 4.5 V, V_{IN} = 0.4 V, other inputs are open.
I_{OS}	Output Short Circuit Current	− 30	− 130	− 30	− 130	− 30	− 130	mA	V_{CC} = 5.5 V, V_{IN} = GND, all other inputs are open, V_{OUT} = GND, S & $\overline{EO}$ = GND.
I_{OZH}	Output Off Current High		20		20		20	µA	V_{CC} = 5.5 V, V_{IN} = 2.0 V, all other inputs are open, V_{OUT} = 2.7 V, $\overline{EO}$ & S = 2.0 V.
I_{OZL}	Output Off Current Low		− 20		− 20		− 20	µA	V_{CC} = 5.5 V, V_{IN} = 0.7 V, V_{OUT} = 0.4 V, S = 0.7 V, $\overline{EO}$ = 2.0 V.
I_{CCH}	Power Supply Current		15		15		15	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs), $\overline{EO}$ = GND.
I_{CCL}	Power Supply Current		9.0		9.0		9.0	mA	V_{CC} = 5.5 V, all inputs are GND.
I_{CCZ}	Power Supply Current		19		19		19	mA	V_{CC} = 5.5 V, all inputs are GND, $\overline{EO}$ = 5.5 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.4 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output Data to Output	3.0 —	23 18	3.0 —	35 30	3.0 —	35 30	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 45 pF.
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output Data to Output	3.0 —	23 18	3.0 —	35 30	3.0 —	35 30	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 45 pF.
t_{PHL5} t_{PHL5}	Propagation Delay /Data-Output Select to Output	3.0 —	26 21	3.0 —	39 34	3.0 —	39 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 45 pF.
t_{PLH5} t_{PLH5}	Propagation Delay /Data-Output Select to Output	3.0 —	26 21	3.0 —	39 34	3.0 —	39 34	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 45 pF.
t_{PZH3} t_{PZH3}	Propagation Delay /Data-Output Output High-Low	3.0 —	35 30	3.0 —	53 48	3.0 —	53 48	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω..
t_{PZL3} t_{PZL3}	Propagation Delay /Data-Output Output High-Low	3.0 —	35 30	3.0 —	53 48	3.0 —	53 48	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 45 pF, R_L = 667 Ω.
t_{PHZ3} t_{PHZ3}	Propagation Delay /Data-Output Output High-Low	3.0 —	35 30	3.0 —	53 48	3.0 —	53 48	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 5.0 pF, R_L = 667 Ω.
t_{PLZ3} t_{PLZ3}	Propagation Delay /Data-Output Output Low-High	3.0 —	30 25	3.0 —	45 40	3.0 —	45 40	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 5.0 pF, R_L = 667 Ω.