Data Sheet July 1999 File Number 2836.4

3A, 80V, 0.800 Ohm, Logic Level, N-Channel Power MOSFETs

The RFD3N08L and RFD3N08LSM are N-Channel enhancement mode silicon gate power field effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V to 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

Formerly developmental type TA09922.

Ordering Information

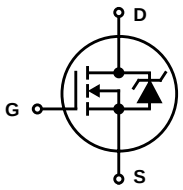
PART NUMBER	PACKAGE	BRAND
RFD3N08L	TO-251AA	F3N08L
RFD3N08LSM	TO-252AA	F3N08L

NOTE: When ordering, include the entire part number. Add the suffix 9A to obtain the TO-252AA variant in tape and reel, i.e. RFD3N08LSM9A

Features

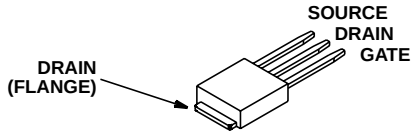
- 3A, 80V
- $r_{DS(ON)} = 0.800\Omega$
- Temperature Compensating PSPICE® Model
- On Resistance vs Gate Drive Voltage Curves
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

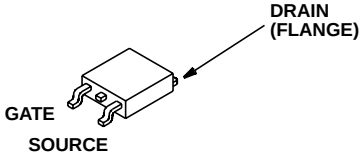


Packaging

JEDEC TO-251AA



JEDEC TO-252AA



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFD3N08L, RFD3N08LSM	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	80	V
Drain to Gate Voltage (R_{GS} = 20KΩ) (Note 1)	V_{DGR}	80	V
Gate to Source Voltage	V_{GS}	±10	V
Continuous Drain Current	I_D	3	A
Pulsed Drain Current (Figures 3, 5) (Note 3)	I_{DM}	Refer to Peak Current Curve	
Maximum Power Dissipation	P_D	30	W
Derate Above 25^oC		0.2	$W/^oC$
Pulsed Avalanche Energy Rating (Figure 6) (Note 4)	E_{AS}	Refer to UIS Curve	
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 12)		80	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA (Figure 11)		1	-	2.5	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V		-	-	25	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V 125^oC		-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±10V		-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 3A, V_{GS} = 5V, (Figures 9, 10)		-	-	0.800	Ω
Turn-On Time	$t_{(ON)}$	V_{DD} = 40V, I_D = 3A, R_L = 13.3Ω, V_{GS} = 5V, R_G = 25Ω, (Figures 13, 15, 18, 19)		-	-	75	ns
Turn-On Delay Time	$t_{d(ON)}$			-	15	-	ns
Rise Time	t_r			-	45	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	22	-	ns
Fall Time	t_f			-	15	-	ns
Turn-Off Time	$t_{(OFF)}$			-	-	45	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 64V, I_D = 3A, $I_{g(REF)}$ = 0.1mA R_L = 21.3Ω (Figures 15, 20, 21)	-	6.8	8.5	nC
Gate Charge at 5V	$Q_{g(5)}$	V_{GS} = 0V to 5V		-	3.8	4.8	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 1V		-	0.18	0.24	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz, (Figure 14)		-	-	125	pF
Output Capacitance	C_{OSS}			-	-	55	pF
Reverse Transfer Characterisics	C_{RSS}			-	-	15	pF
Thermal Resistance, Junction to Case	$R_{\theta JC}$			-	-	5.0	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$			-	-	100	$^oC/W$

Source to Drain Diode Ratings and Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = 3A	-	-	1.25	V
Reverse Recovery Time	t_{rr}	I_{SD} = 3A, dI_{SD}/dt = 100A/μs	-	-	85	ns

NOTES:

2. Pulsed: pulse duration = 300μs max, duty cycle = 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. Refer to Intersil Application Notes AN9321 and AN9322.

Typical Performance Curves Unless Otherwise Specified

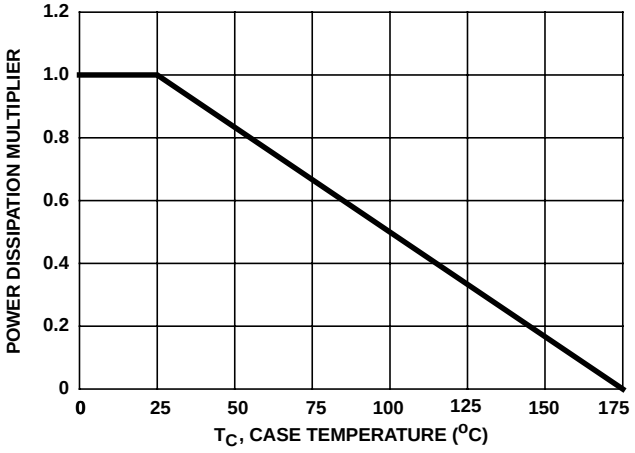


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

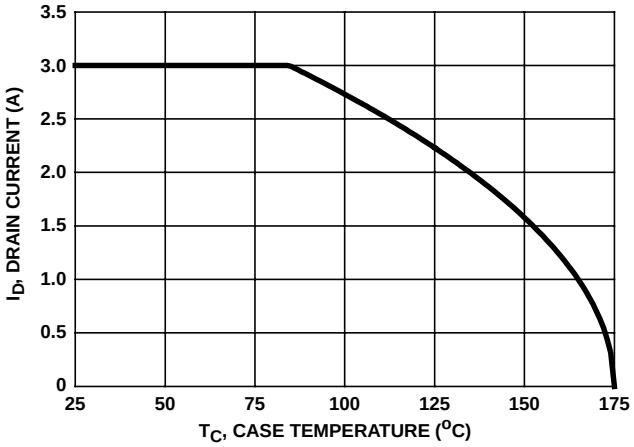


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

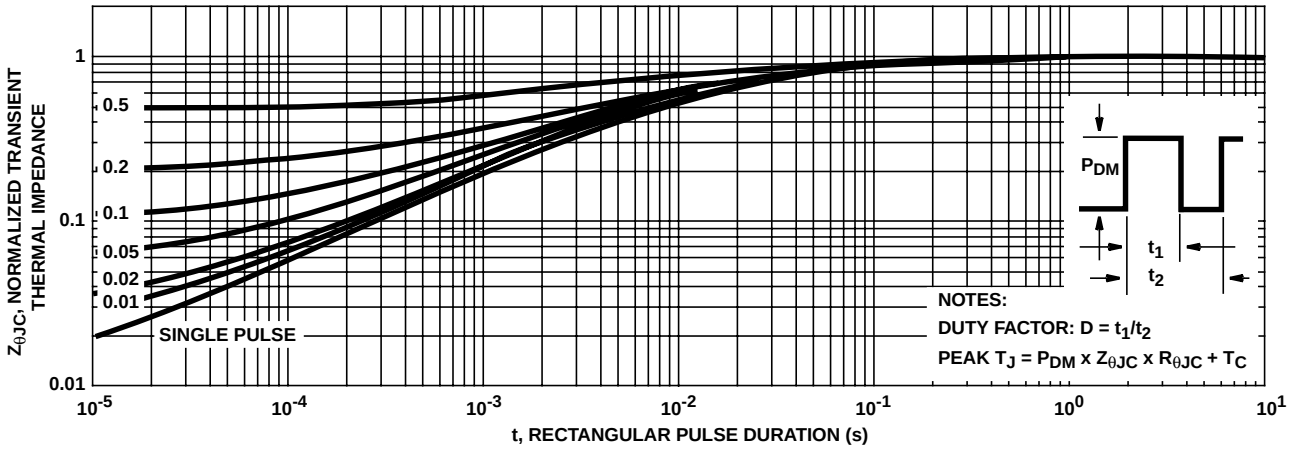


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

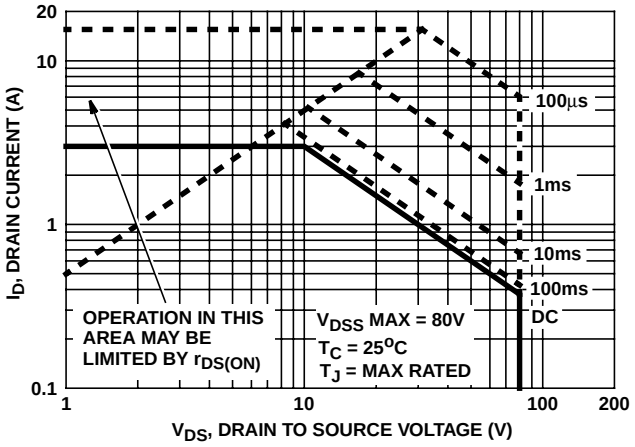


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

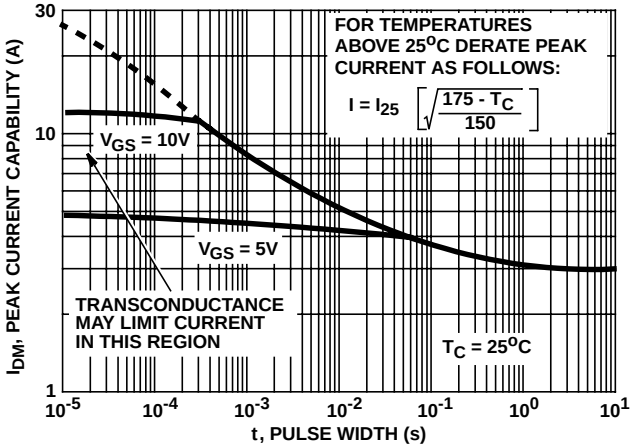
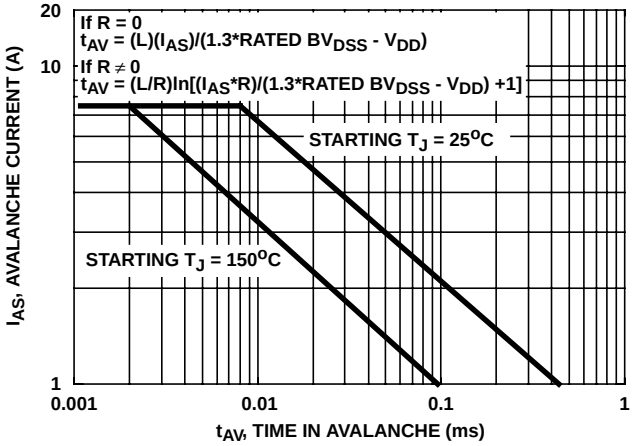


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

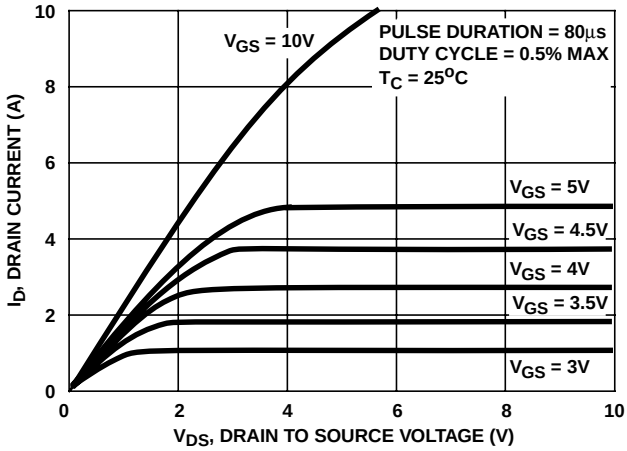


FIGURE 7. SATURATION CHARACTERISTICS

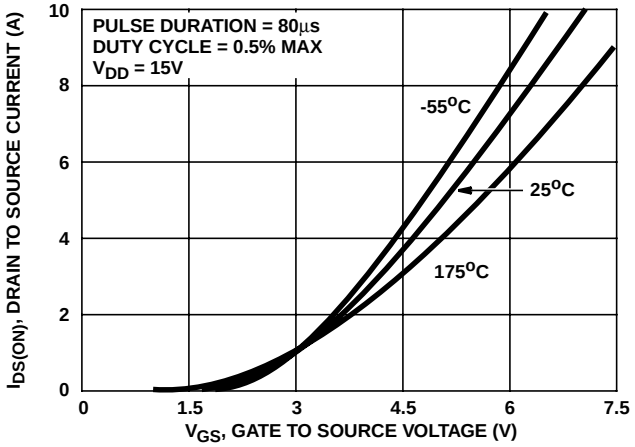


FIGURE 8. TRANSFER CHARACTERISTICS

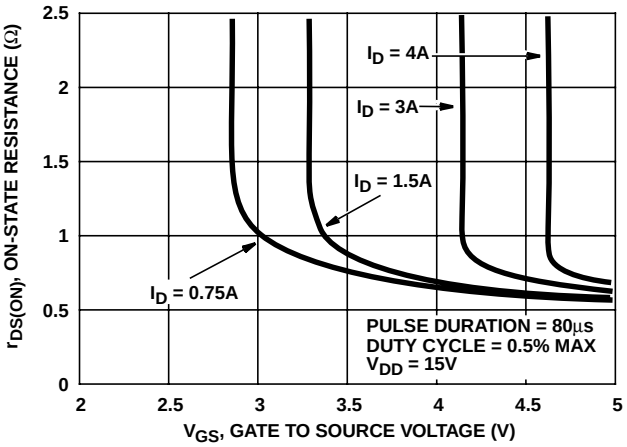


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

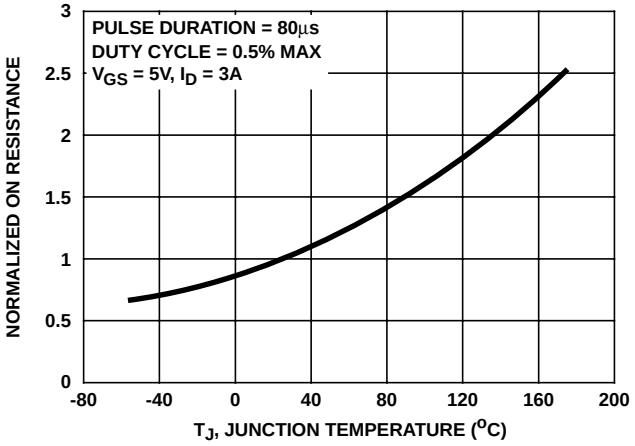


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

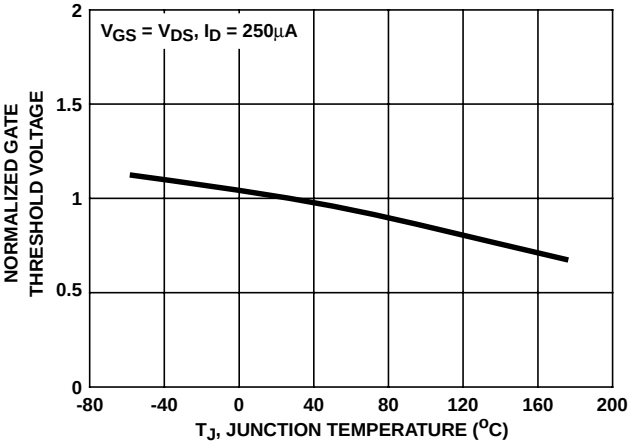


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified **(Continued)**

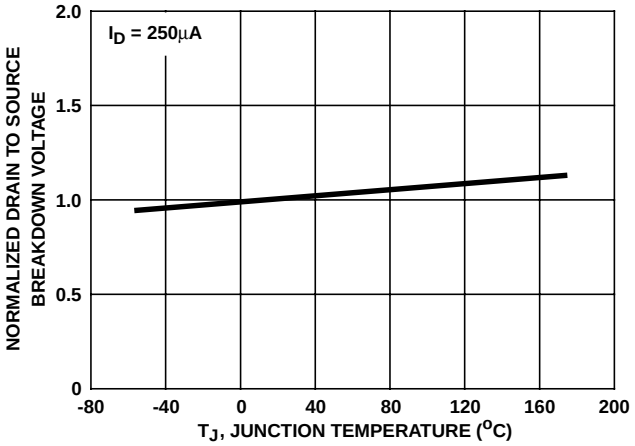


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

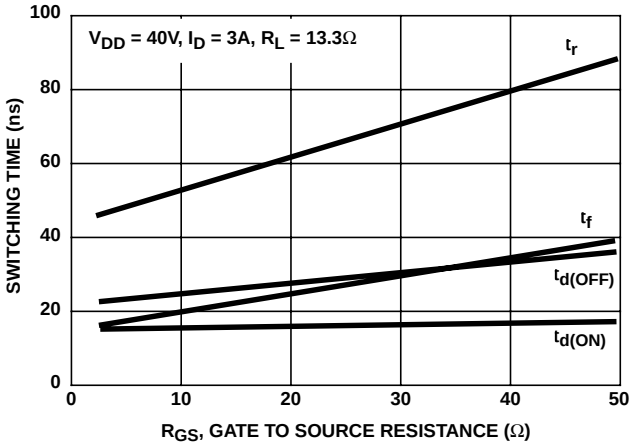


FIGURE 13. SWITCHING TIME vs GATE RESISTANCE

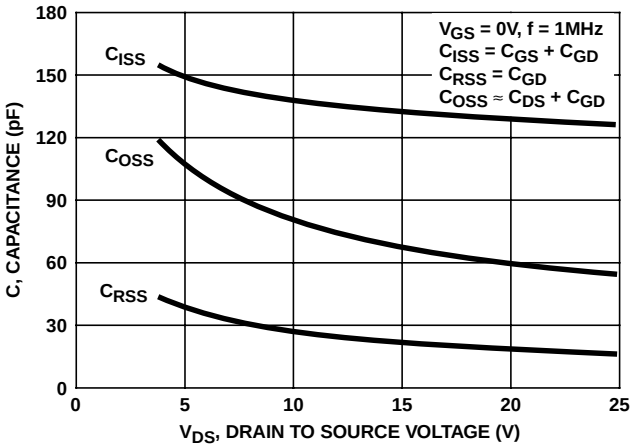
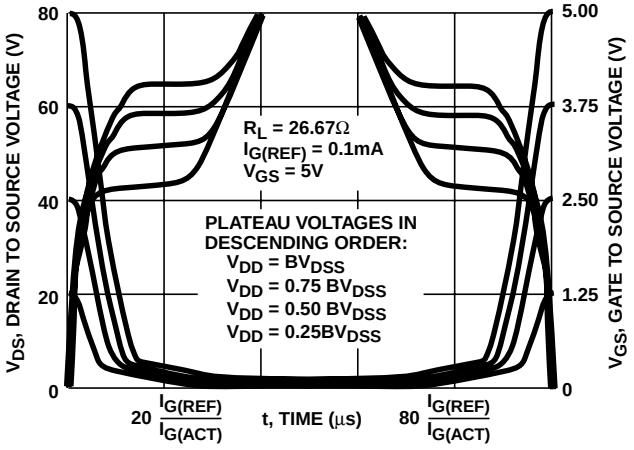


FIGURE 14. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 15. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

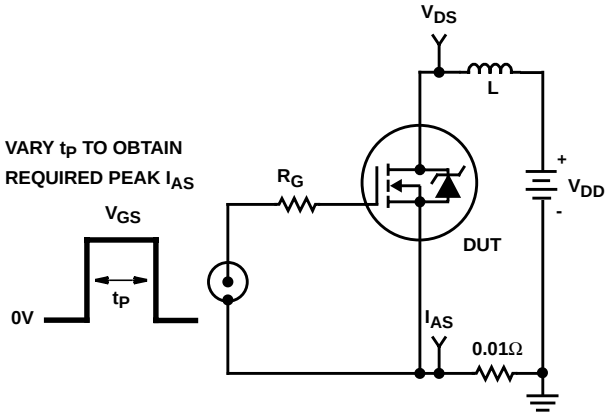


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

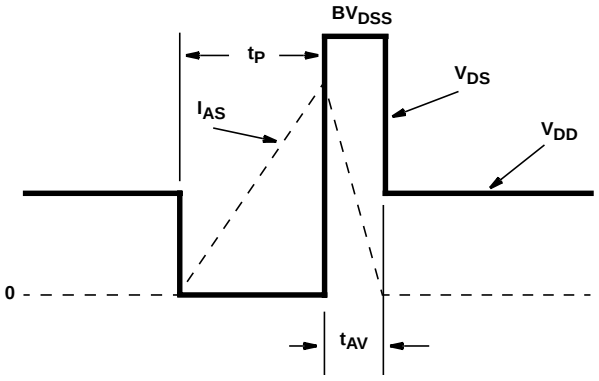


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

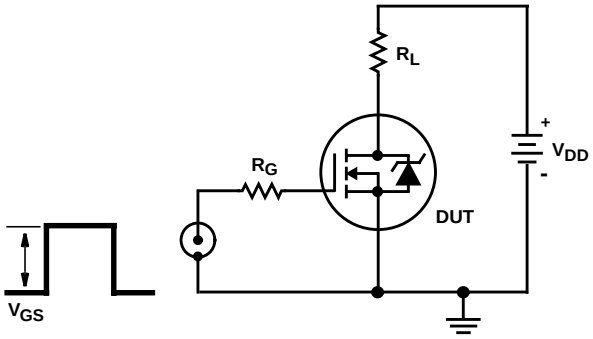


FIGURE 18. SWITCHING TIME TEST CIRCUIT

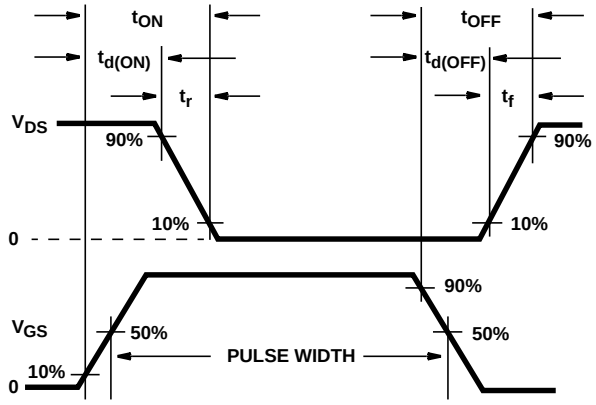


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

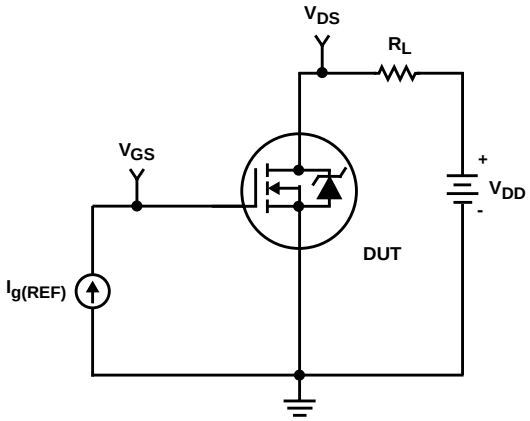


FIGURE 20. GATE CHARGE TEST CIRCUIT

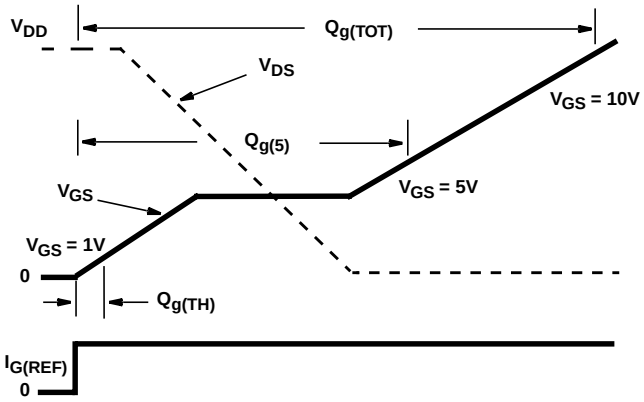
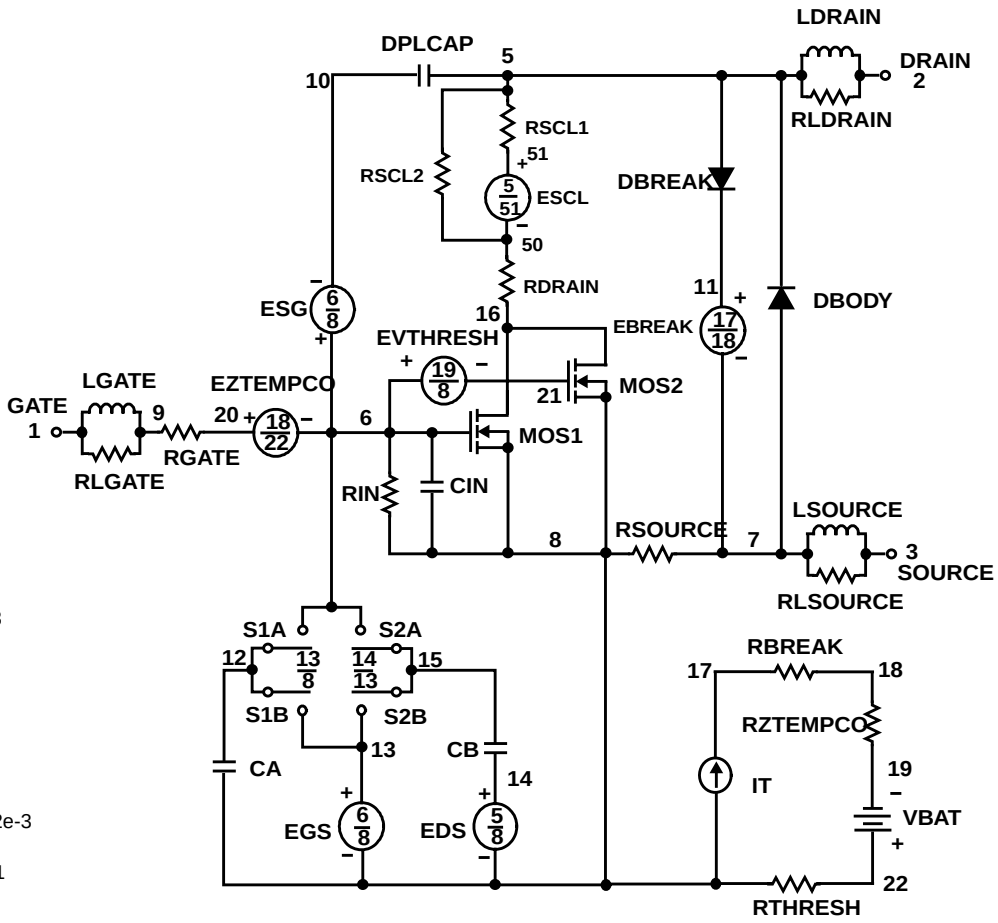


FIGURE 21. GATE CHARGE WAVEFORMS

PSPICE Electrical Model

SUBCKT RFD3N08L 2 1 3 ; rev 5/10/95

```
CA  12  8  4.10e-10
CB  15  14  3.25e-10
CIN  6  8  1.10e-10

DBODY  7  5  DBDMOD
DBREAK  5 11  DBREAKMOD
DPLCAP 10  5  DPLCAPMOD

EBREAK  11  7  17  18  93.57
EDS  14  8  5  8  1
EGS  13  8  6  8  1
ESG  6  10  6  8  1
EVTHRESH  6  21  19  8  1
EZTEMPCO  20  6  18  22  1

IT  8  17  1

LDRAIN  2  5  1e-9
LGATE  1  9  5.8e-9
LSOURCE  3  7  5.8e-9

MOS1  16  6  8  8  MSTRONG  M = 0.80
MOS2  16  21  8  8  MWEAK  M = 0.20

RBREAK  17  18  RBREAKMOD  1
RDRAIN  50  16  RDRAINMOD  174.2e-3
RGATE  9  20  24.9
RIN  6  8  1e9
RLDRAIN  2  5  10
RLGATE  1  9  58
RLSOURCE  3  7  58
RSCL1  5  51  RSCLMOD  1e-6
RSCL2  5  50  1e3
RSOURCE  8  7  RSOURCEMOD  200.2e-3
RTHRESH  22  8  RTHRESHMOD  1
RZTEMPCO  18  19  RZTEMPCOMOD  1

S1A  6  12  13  8  S1AMOD
S1B  13  12  13  8  S1BMOD
S2A  6  15  14  13  S2AMOD
S2B  13  15  14  13  S2BMOD

VBAT  22  19  DC  1

ESCL  51  50  VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*10),6))}

.MODEL DBDMOD D (IS = 9.90e-14  RS = 6.00e-2  TRS1 = 1.42e-3  TRS2 = -3.58e-6  CJO = 1.40e-10  TT = 5.75e-8  M = 0.4)
.MODEL DBREAKMOD D (RS = 2.32  TRS1 = 1.03e-3  TRS2 = -6.17e-11)
.MODEL DPLCAPMOD D (CJO = 1.13e-10  IS = 1e-30  N = 10  M=0.6)
.MODEL MSTRONG NMOS (VTO = 1.773  KP = 1.70  IS = 1e-30  N = 10  TOX = 1L = 1u  W = 1u)
.MODEL MWEAK NMOS (VTO = 1.496  KP = 2.09 IS = 1e-30  N = 10  TOX = 1L = 1u  W = 1u)
.MODEL RBREAKMOD RES (TC1 = 8.19e-4  TC2 = 5.9e-7)
.MODEL RDRAINMOD RES (TC1 = 1.55e-2  TC2 = 8.58e-5)
.MODEL RDSOURCEMOD RES (TC1 = 0  TC2 = 0)
.MODEL RSCLMOD RES (TC1 = 0  TC2 = 0)
.MODEL RTHRESHMOD RES (TC1 = -5.0e-4  TC2 = -6.0e-6)
.MODEL RZTEMPCOMOD RES (TC1 = -1.19e-3  TC2 = 1.12e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -5.2  VOFF= -3.2)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -3.2  VOFF= -5.2)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -0.60  VOFF= 4.4)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 4.4  VOFF= -0.60)

.ENDS
```



NOTE:

1. For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET** Featuring Global Temperature Options; IEEE Power Electronics Specialist Conference Records, 1991.

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029